CR-1 8 7 6 5 4 3 (FULL_ID=532-1-8142) (PAGE_INFO_ID=8142) 2 (OWNED_BY=DE) (MODULE_ID=532-1-8142) 1 (DONOR_ID=532-1-8142)

REVISIONS							
REV	DESCRIPTION	DFT	DATE	CHK	DATE	APVD	DATE

DVTM

MECHANICAL

NOTES:

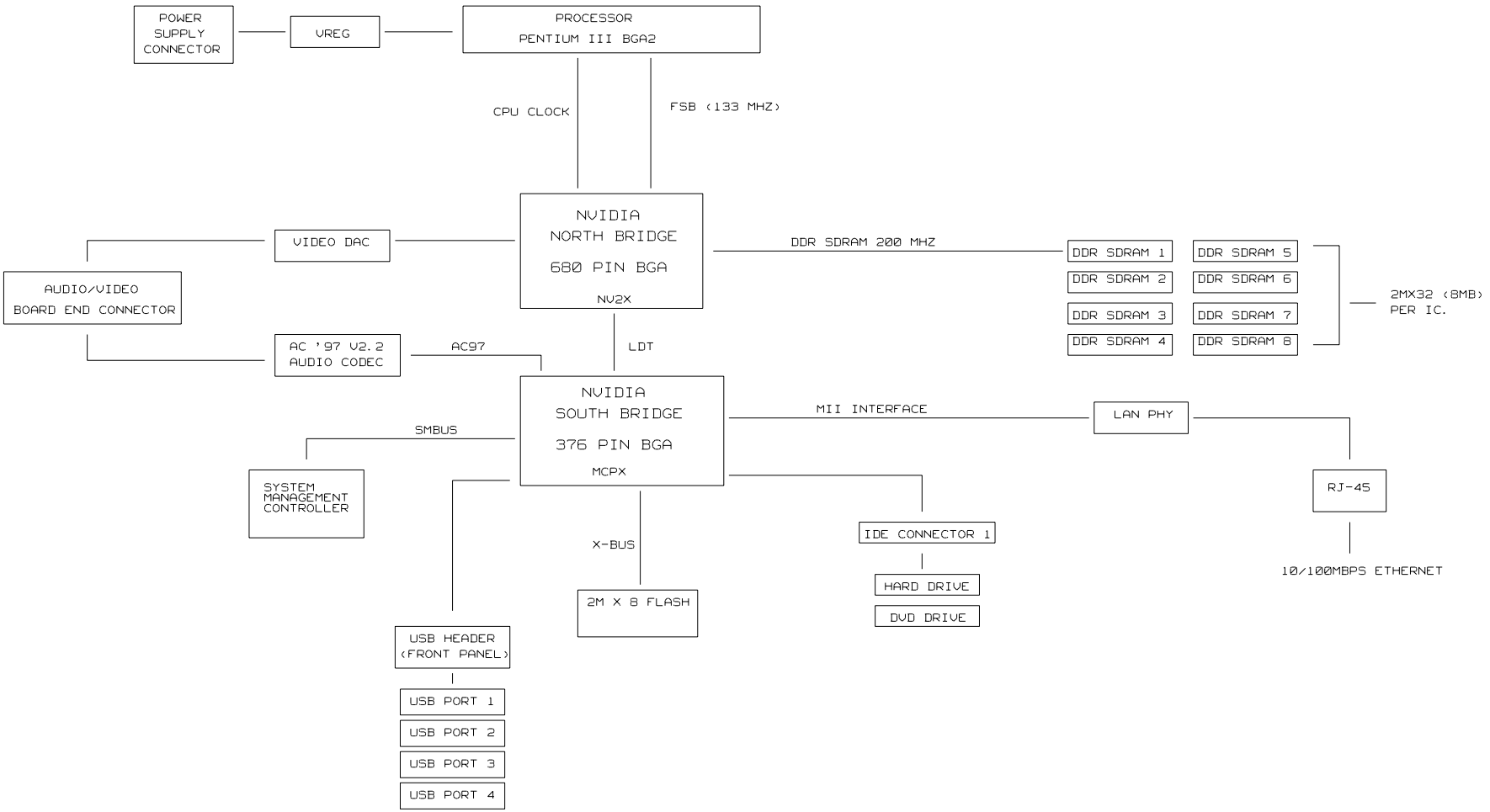
1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPLs FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.

[PAGE_TITLE=COVER PAGE]

DRAWING
DVT.SCH_1.1
Fri Sep 01 08:42:25 2000

BOM RELEASE DATE	xx/xx/xx	PB NUMBER XXXXXX-XXX
SIGNATURE	DATE	intel 3065 BOWERS AVE SANTA CLARA, CA 95051
DRN BY		
CHK BY N_SANCHEZ	xx/xx/xx	TITLE SCH, PBA, DVT
ENGR APVD		
APVD		INTEL CONFIDENTIAL / DOCUMENT NUMBER XXXXXX / PAGE 1/53 / REV 0.13
APVD		

(DONOR_REV=) (DONOR_PROJ=) 8 (PROJ_REV=0.13/page1) (PROJ_NAME=DVT_A--532) 6 (MODULE=NONE) 5 4 (LAST_MAKEPROJ: 9/1/00 8:54:19 AM) 3 2 1

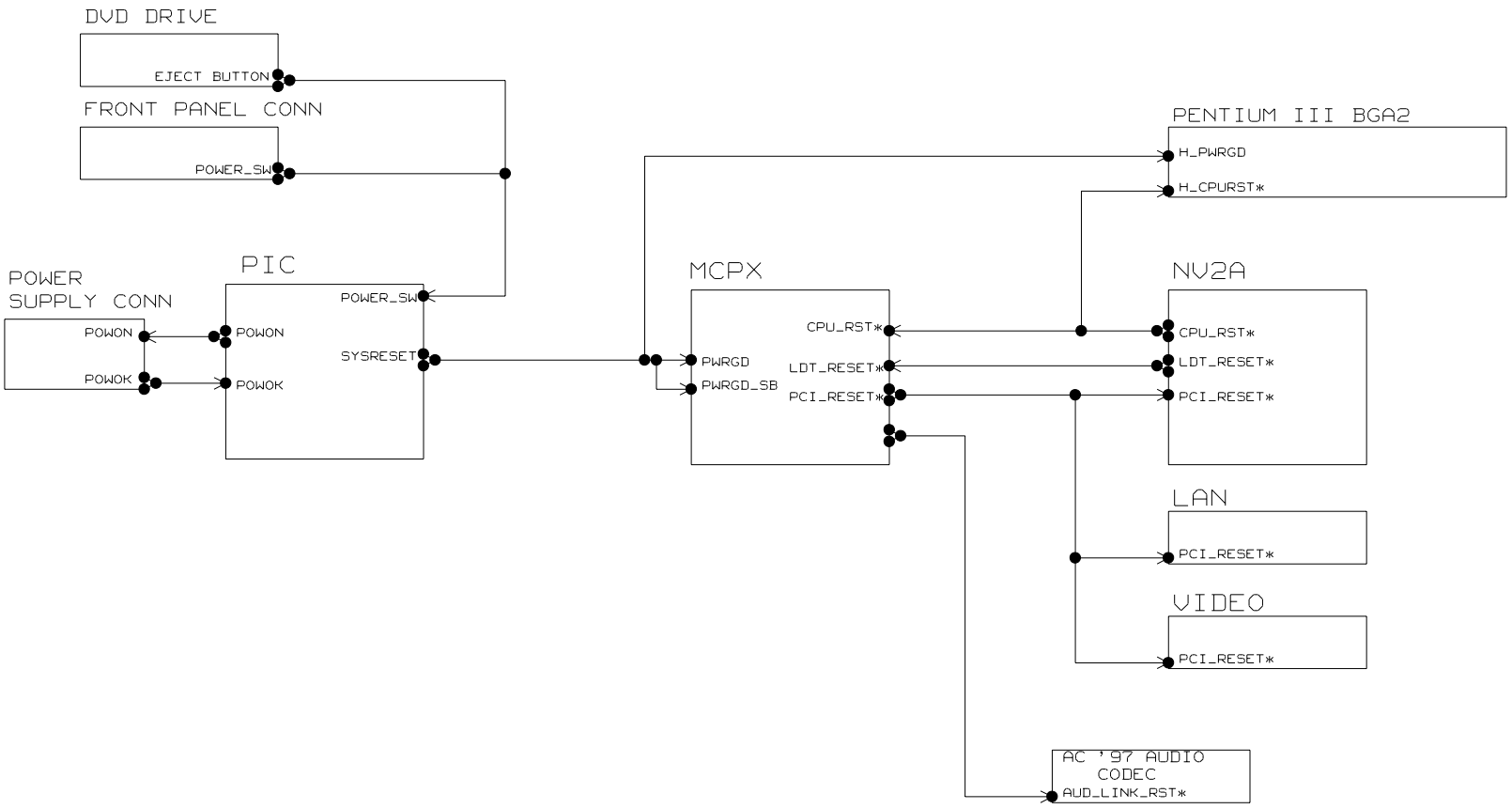


[PAGE_TITLE=BLOCK DIAGRAM]

DRAWING
DVT.SCH_1.2
Fri Sep 01 07:32:12 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	2	0.13

RESET & POWER-ON MAP



[PAGE_TITLE=RESET MAP]

DRAWING
DVT.SCH_1.3
Fri Sep 01 07:32:07 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	3	0.13

TABLES NEED TO BE UPDATED

DEVICE	BUS ID	DEVICE ID	FUNCTION	IDSEL	REQ/GNT	INTERRUPT	APIC
NORTH BRIDGE							
MEMORY CONTROLLER	0	1130	-	-	-	-	-
GPU	0	1131	-	-	-	-	-
	0	1132					
SOUTH BRIDGE							
PCI BRIDGE	0	30	0	N/A	N/A	N/A	N/A
LPC BRIDGE	00	31	0	N/A	N/A	N/A	N/A
IDE CONTROLLER	00	31	1	N/A	N/A	14 OR 15	14
USB CONTROLLER	00	31	2	N/A	N/A	C, D	18
SMBUS CONTROLLER	00	31	3	N/A	N/A	B	17
AC'97-AUD-CONTROLLER		31	5	N/A	N/A	B	17
AC'97-MOD-CONTROLLER		31	6	N/A	N/A	B	17
LAN CONTROLLER		8	0	24	N/A	E	
						A, B	
-DEVICE 0		0		AD16	0		AD16
-DEVICE 1		1		AD17	1		AD17
-DEVICE 2		2		AD18	2		AD18
-DEVICE 3		3		AD19	3		AD19
-DEVICE 4		4		AD20	4		AD20
-DEVICE 5		5		AD21	5		AD21
-DEVICE 6		6		AD22	6		AD22
-DEVICE 7		7		AD23	7		AD23
-DEVICE 8		8		AD24	8		AD24
-DEVICE 9		9		AD25	9		AD25
-DEVICE 10		10		AD26	10		AD26
-DEVICE 11		11		AD27	11		AD27
-DEVICE 12		12		AD28	12		AD28
-DEVICE 13		13		AD29	13		AD29
-DEVICE 14		14		AD30	14		AD30
-DEVICE 15		15		AD31	15		AD31

IDSEL TABLE

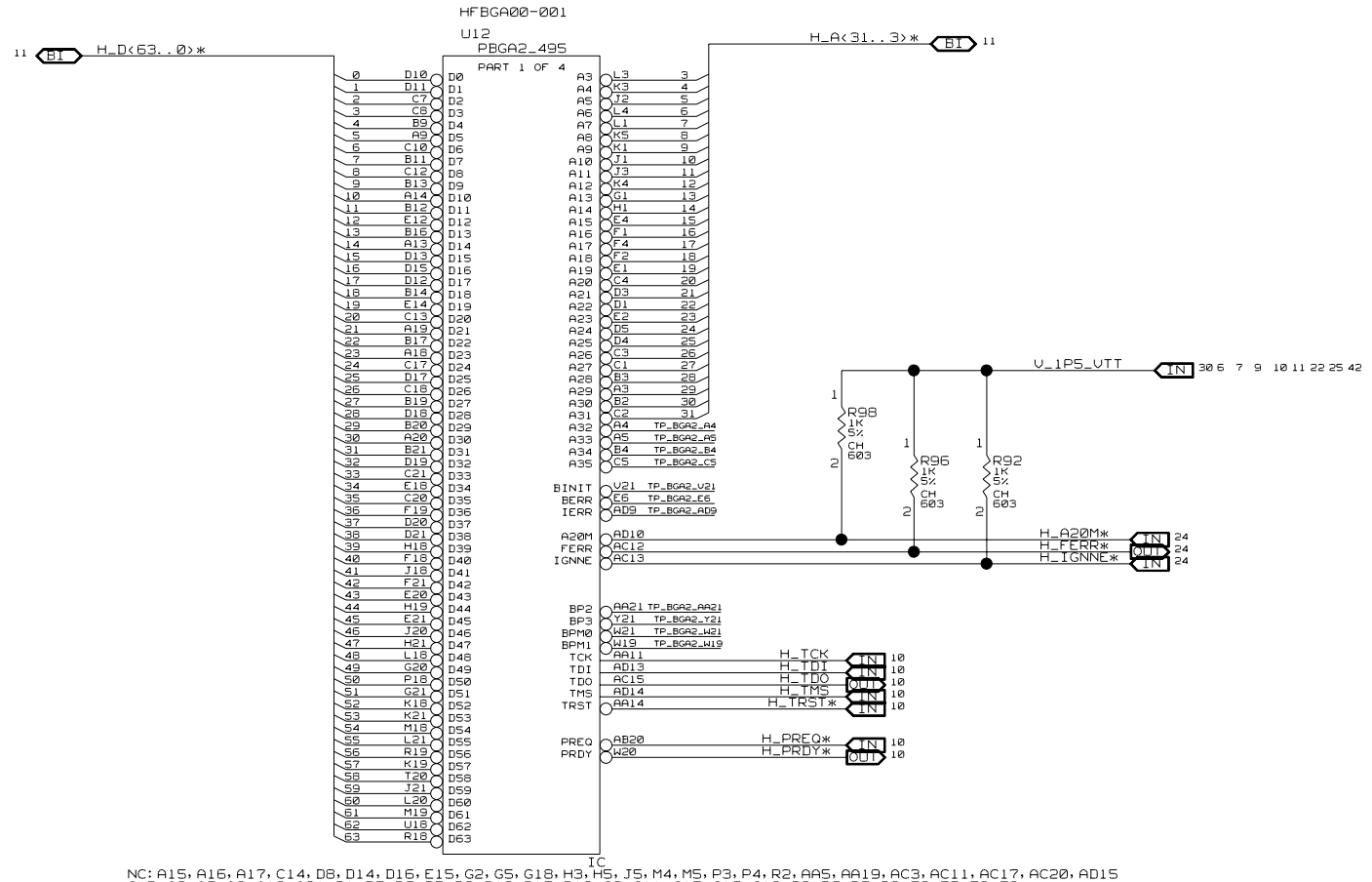
DEVICE	NAME	I/O	POWER WELL	DURING RESET	AFTER RESET	USAGE
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						
MCPX						

GPIO USAGE TABLE

[PAGE_TITLE=GPIO/IDSEL TABLE]

DRAWING
DVT.SCH_1.4
Fri Sep 01 07:32:03 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	4	0.13



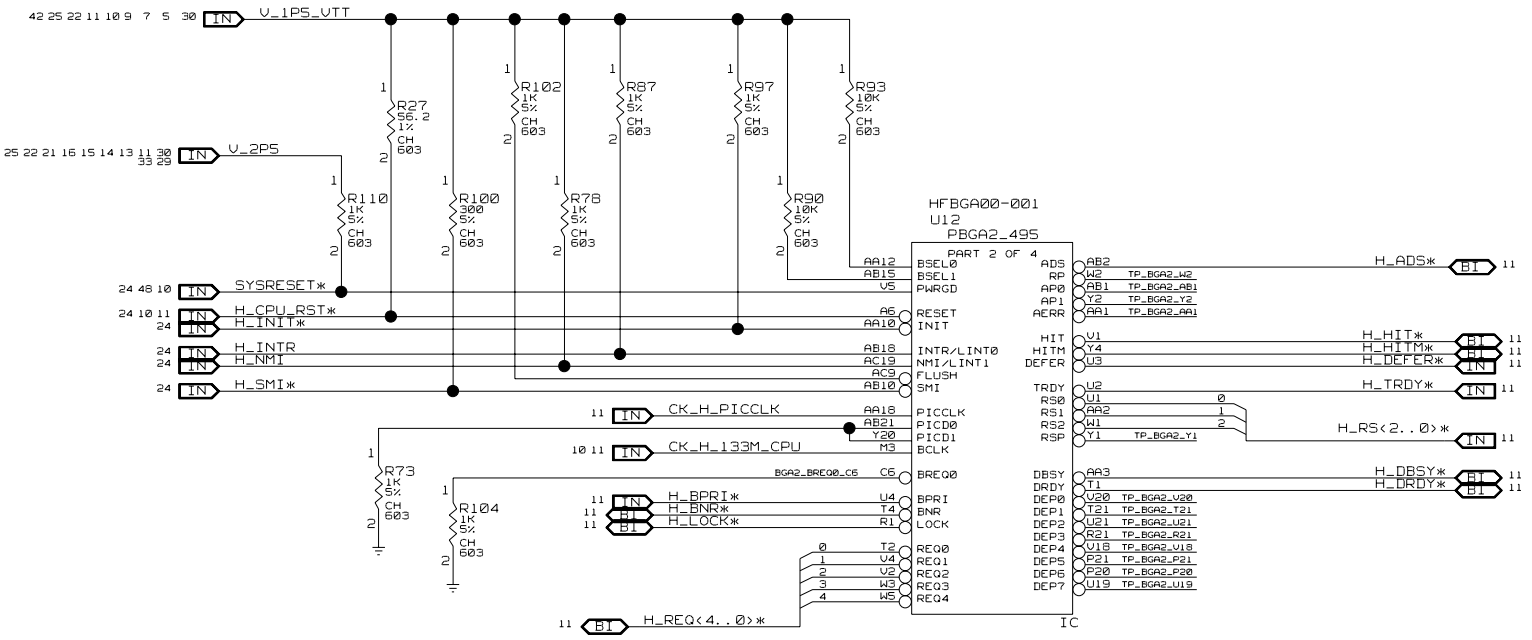
NC: A15, A16, A17, C14, D8, D14, D16, E15, G2, G5, G18, H3, H5, J5, M4, M5, P3, P4, R2, AA5, AA19, AC3, AC11, AC17, AC20, AD15
GND: A2, A7, A8, A12, A21, B1, B5, B6, B7, B8, B10, B15, B18, C9, C11, C15, C16, C19, D2, D6, D7, D9, E3, E7, E8, E9
GND: E10, E11, E13, E19, F3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F20, G3, G19, H2, H7, H9, H11, H13, H15
GND: H20, J4, J8, J10, J12, J14, J16, J19, K2, K7, K9, K11, K13, K15, K20, L5, L8, L10, L12, L14, L16, L19, M7, M9, M11
GND: M13, M15, M20, N2, N3, N4, N8, N10, N12, N14, N16, N18, N19, N20, P5, P7, P9, P11, P13, P15, P19, R3, R4, R5, R8, R10, R12, R14, R16, R20
GND: T3, T5, T7, T9, T11, T13, T15, T18, T19, U8, U10, U12, U14, U16, U20, V3, V19, W4, W18, Y3, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y19
GND: AA4, AA13, AA20, AB3, AB5, AB9, AB11, AB13, AB14, AB17, AC1, AC2, AC5, AC10, AC14, AC16, AC21, AD1, AD5, AD16, AD21, AC18

[PAGE_TITLE=PENTIUM III BGA2 PART 1 OF 4]

DRAWING
DVT.SCH_1.5
Fri Sep 01 07:31:58 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	5	0.13

BSEL1	BSEL0	SYSTEM BUS FREQUENCY
0	0	66 MHZ
0	1	100 MHZ
1	0	RESERVED
1	1	133 MHZ

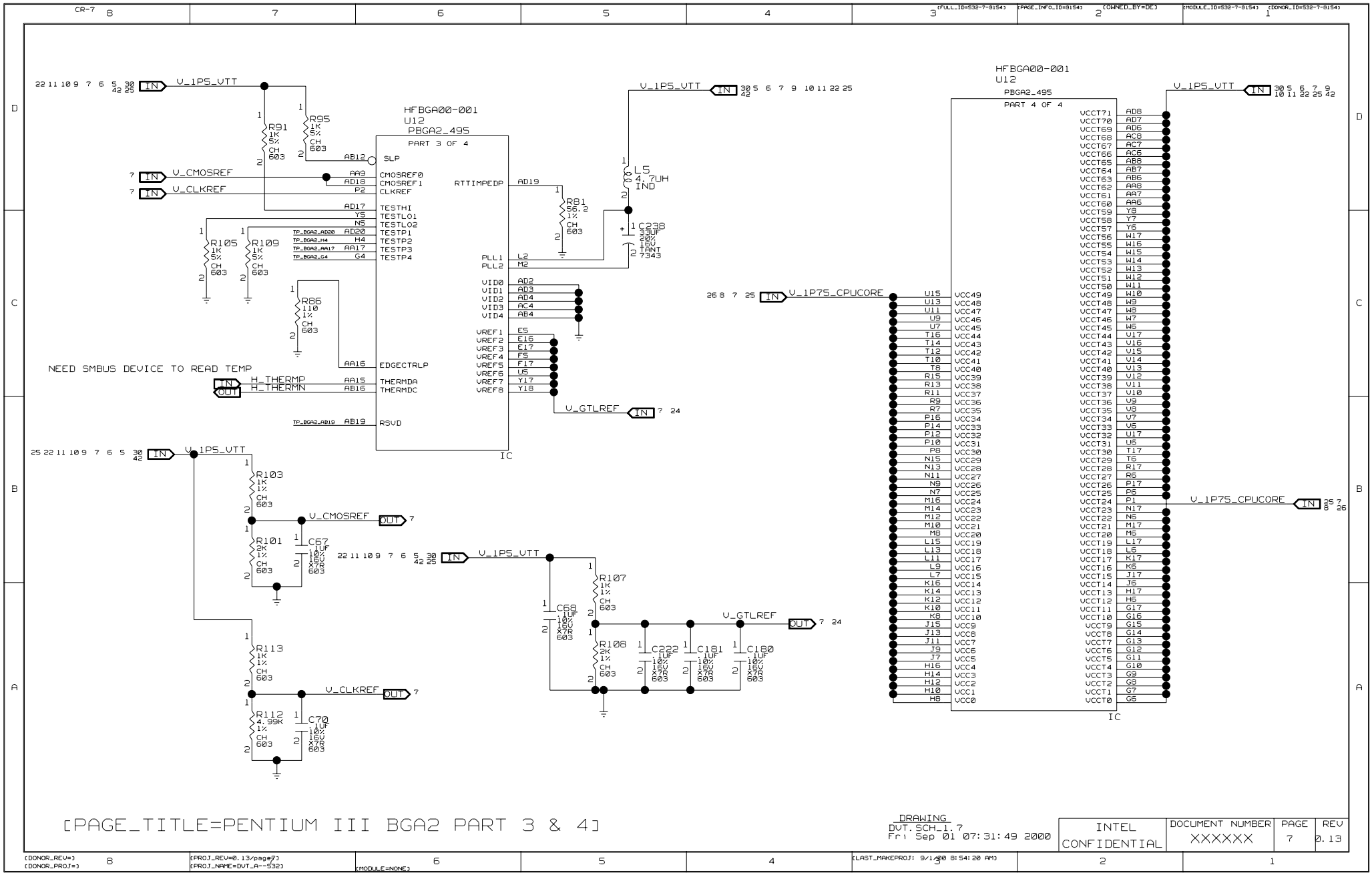


NC: A15, A16, A17, C14, D8, D14, D16, E15, G2, G5, G18, H3, H5, J5, M4, M5, P3, P4, R2, AA5, AA19, AC3, AC11, AC17, AC20, AD15
GND: A2, A7, A8, A12, A21, B1, B5, B6, B7, B8, B10, B15, B18, C9, C11, C15, C16, C19, D2, D6, D7, D9, E3, E7, E8, E9
GND: E10, E11, E13, E19, F3, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, F20, G3, G19, H2, H7, H9, H11, H13, H15
GND: H20, J4, J8, J10, J12, J14, J16, J19, K2, K7, K9, K11, K13, K15, K20, L5, L8, L10, L12, L14, L16, L19, M7, M9, M11
GND: M13, M15, M20, N2, N3, N4, N8, N10, N12, N14, N16, N18, N19, N20, P5, P7, P9, P11, P13, P15, P19, R3, R4, R5, R8, R10, R12, R14, R16, R20
GND: T3, T5, T7, T9, T11, T13, T15, T18, T19, U8, U10, U12, U14, U16, U20, V3, V19, W4, W18, Y3, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y19
GND: AA4, AA13, AA20, AB3, AB5, AB9, AB11, AB13, AB14, AB17, AC1, AC2, AC5, AC10, AC14, AC16, AC21, AD1, AD5, AD16, AD21, AC18

[PAGE_TITLE=PENITUM III BGA2 PART 2 OF 4]

DRAWING
DVT.SCH_1.6
Fri Sep 01 07:31:54 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	6	0.13



[PAGE_TITLE=PENTIUM III BGA2 PART 3 & 4]

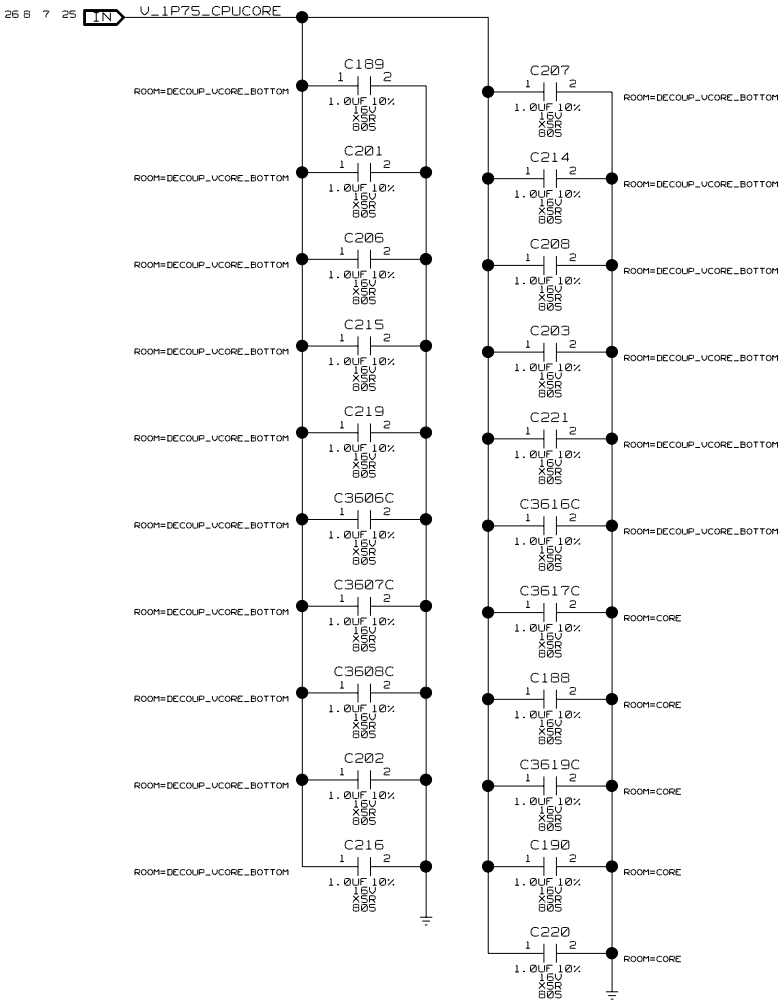
DRAWING
DVT.SCH_1.7
Fri Sep 01 07:31:49 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	7	0.13

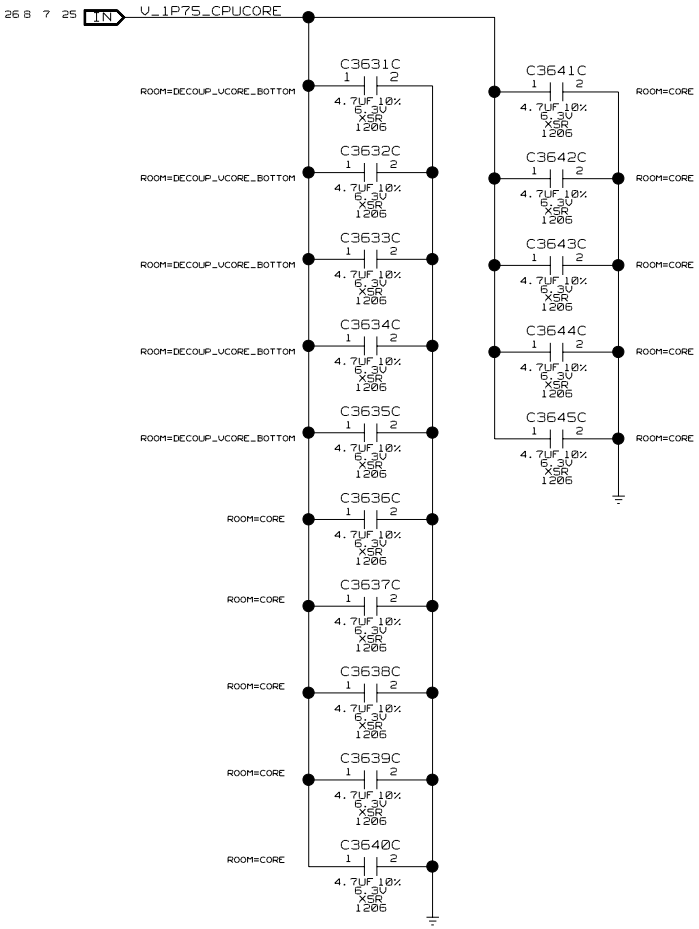
[DONOR_REV=]
[DONOR_PROJ=]
[PROJ_REV=0.13/page7]
[PROJ_NAME=DVT_A--532]
[MODULE=NONE]
[LAST_MAKEPROJ: 9/1/00 8:54:20 AM]

CPU VCORE DECOUPLING

16 1.0UF CAPS PLACED ON BOTTOM.
5 1.0UF CAPS PLACED ON TOP.



5 4.7UF CAPS PLACED ON BOTTOM.
10 4.7UF CAPS PLACED ON TOP.



[PAGE_TITLE=CPU VCORE DECOUPLING]

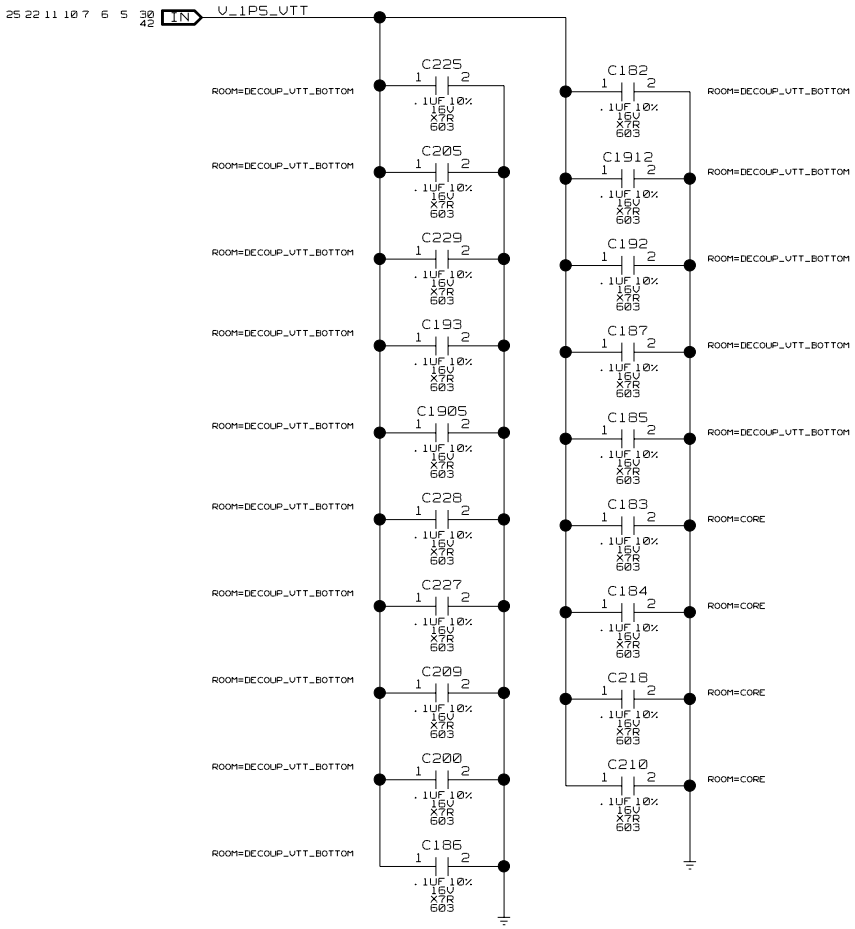
CPU VCORE DECOUPLING

DRAWING
DVT.SCH_1.8
Fri Sep 01 07:31:45 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	8	0.13

CPU VTT DECOUPLING CAPS

15 PLACED ON BOTTOM OF CPU.



[PAGE_TITLE=CPU VTT DECPUPLING]

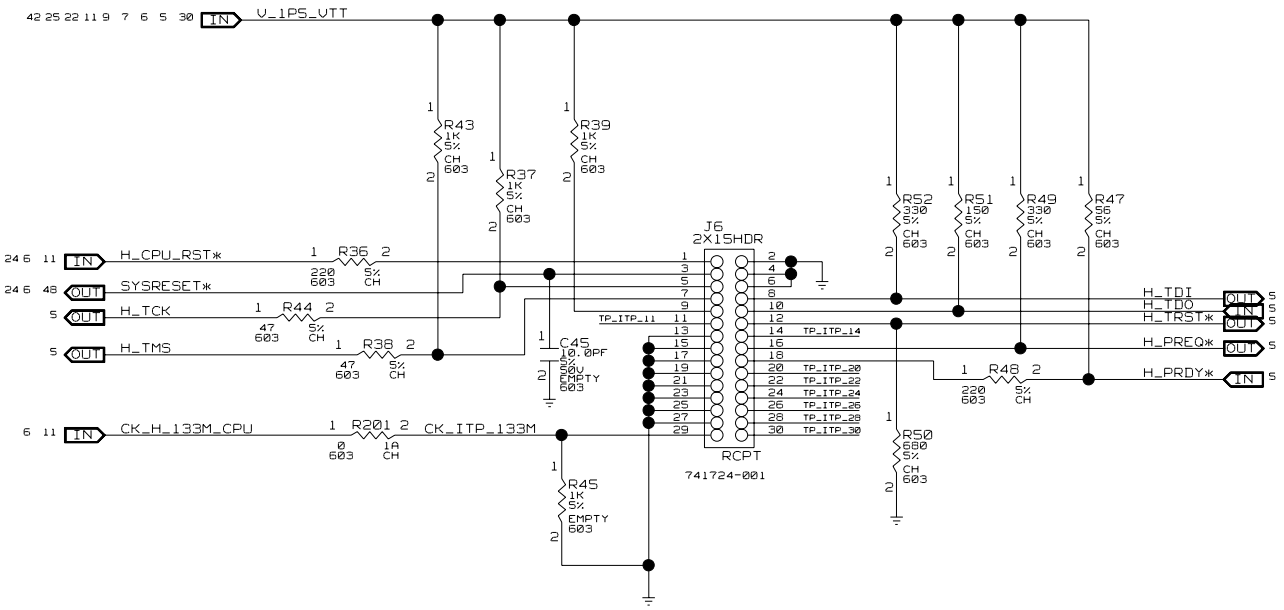
DRAWING
DVT.SCH_1.9
Fri Sep 01 07:31:40 2000

CPU VTT DECOUPLING

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	9	0.13

CR-10

CUMINE ITP VERSION

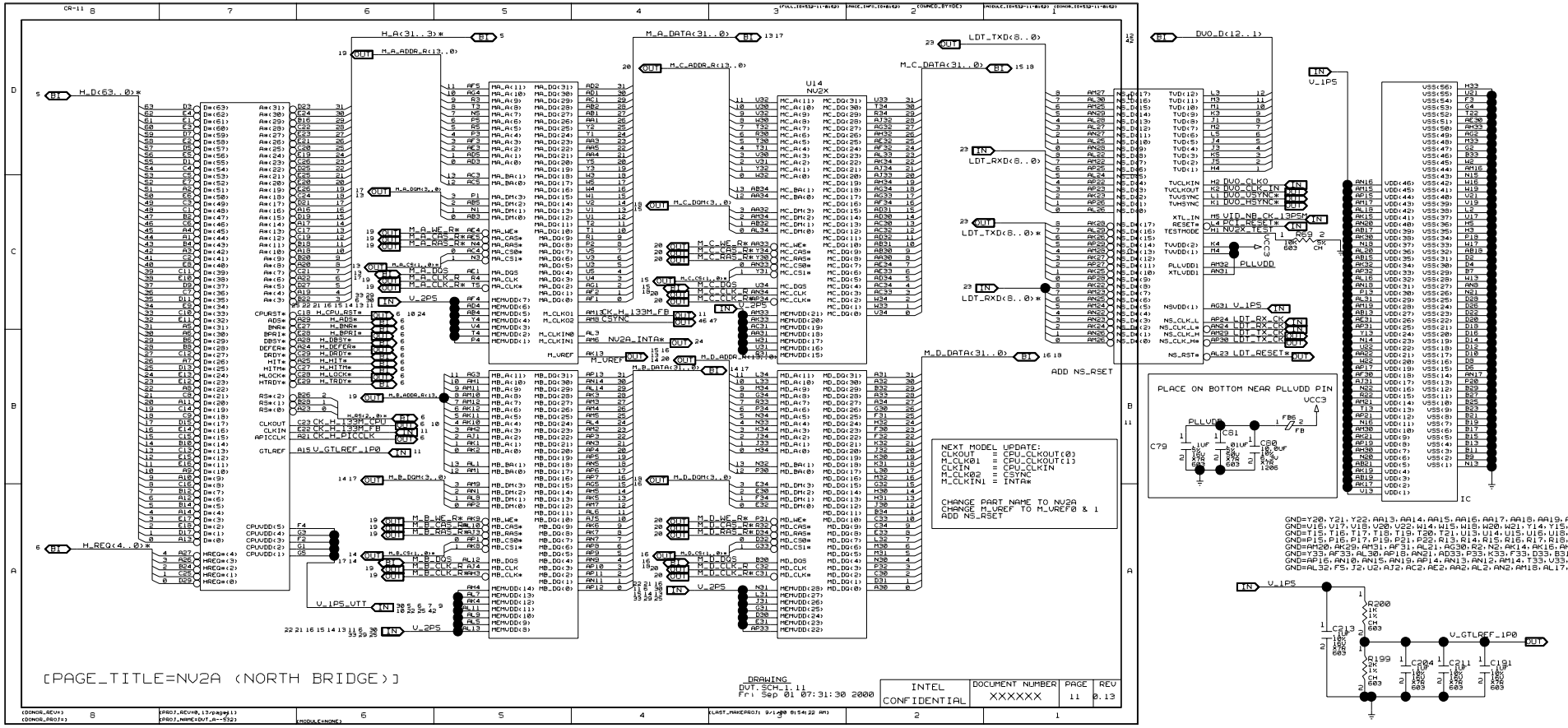


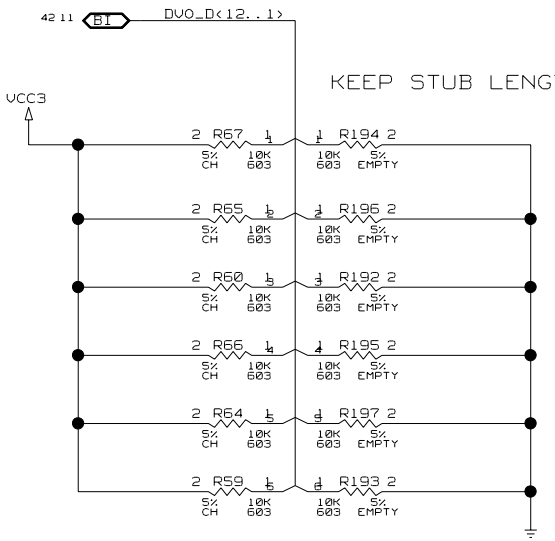
[PAGE_TITLE=ITP CONNECTOR]

DRAWING
DVT.SCH_1.10
Fri Sep 01 07:31:35 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	10	0.13

[DONOR_REV=]
[DONOR_PROJ=]
[PROJ_REV=0.13/page=10]
[PROJ_NAME=DVT_A--532]
[MODULE=NONE]
[LAST_MAKEPROJ: 9/1/00 8:54:21 AM]
[FULL_ID=532-10-8160] [PAGE_INFO_ID=8160] [OWNED_BY=DE] [MODULE_ID=532-10-8160] [DONOR_ID=532-10-8160]


[PAGE_TITLE=NV2A (NORTH BRIDGE)]
DRAWING
DVT.SCH_1.11
Fri Sep 01 07:31:30 2000
INTEL CONFIDENTIAL
DOCUMENT NUMBER
XXXXXX
PAGE
11
REV
0.13
NEXT MODEL UPDATE:
CLKOUT = CPU_CLKOUT(0)
M_CLK01 = CPU_CLKOUT(1)
CLKIN = CPU_CLKIN
M_CLK02 = CSYNC
M_CLKIN1 = INTA#
CHANGE PART NAME TO NV2A
CHANGE M_VREF TO M_VREF0 & 1
ADD NS_RSET
PLACE ON BOTTOM NEAR PLLVDD PIN
VCC3
PLLVDD
C79
CS1
C80
FB5
FB
IC
GND=Y20,Y21,Y22,AA13,AA14,AA15,AA16,AA17,AA18,AA19,AA20,AA21,AB14,AB16
GND=V16,V17,V18,V20,V22,W14,W15,W18,W20,W21,Y14,Y15,Y16,Y17,Y18,Y19,AB20
GND=T15,T16,T17,T18,T19,T20,T21,U13,U14,U15,U16,U18,U19,U20,V14,V15,F1,B5
GND=F15,P16,P17,P19,P21,P22,R13,R14,R15,R16,R17,R18,R19,R20,R21,T14,AK31
GND=AM20,AK29,AM31,AF31,AL21,AG30,R2,N2,AK14,AK15,AK18,N17,N19,P14,D24
GND=Y33,AF33,AL30,AP18,AN21,AD33,F33,D33,B31,AL19,AP20,AK20,AH31
GND=AP16,AN10,AN15,AN19,AP14,AN13,AN12,AM14,T33,U33,AM29,AJ30,AB33,B1,B3
GND=AL32,F5,J2,U2,AJ2,AC2,AE2,AA2,AL2,AN2,AM18,AL17,AL15,AN4,AN6,AB22

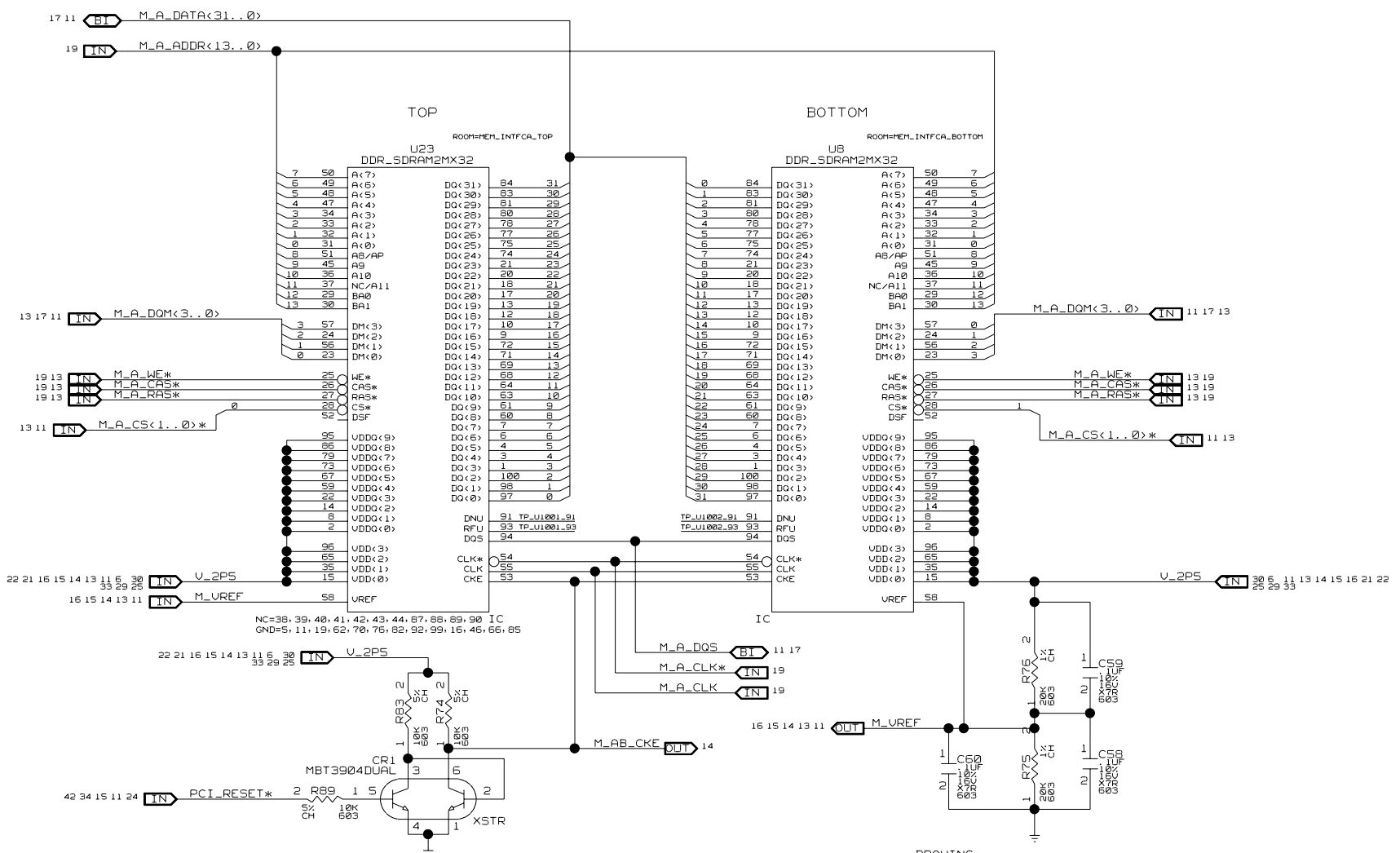


{PAGE_TITLE=NV2A STRAPPING}

DRAWING
DVT.SCH_1.12
Fri Sep 01 07:31:25 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	12	0.13

MEMORY INTERFACE PARTITION A



[PAGE_TITLE=DDR SDRAM (PARTITION A)]

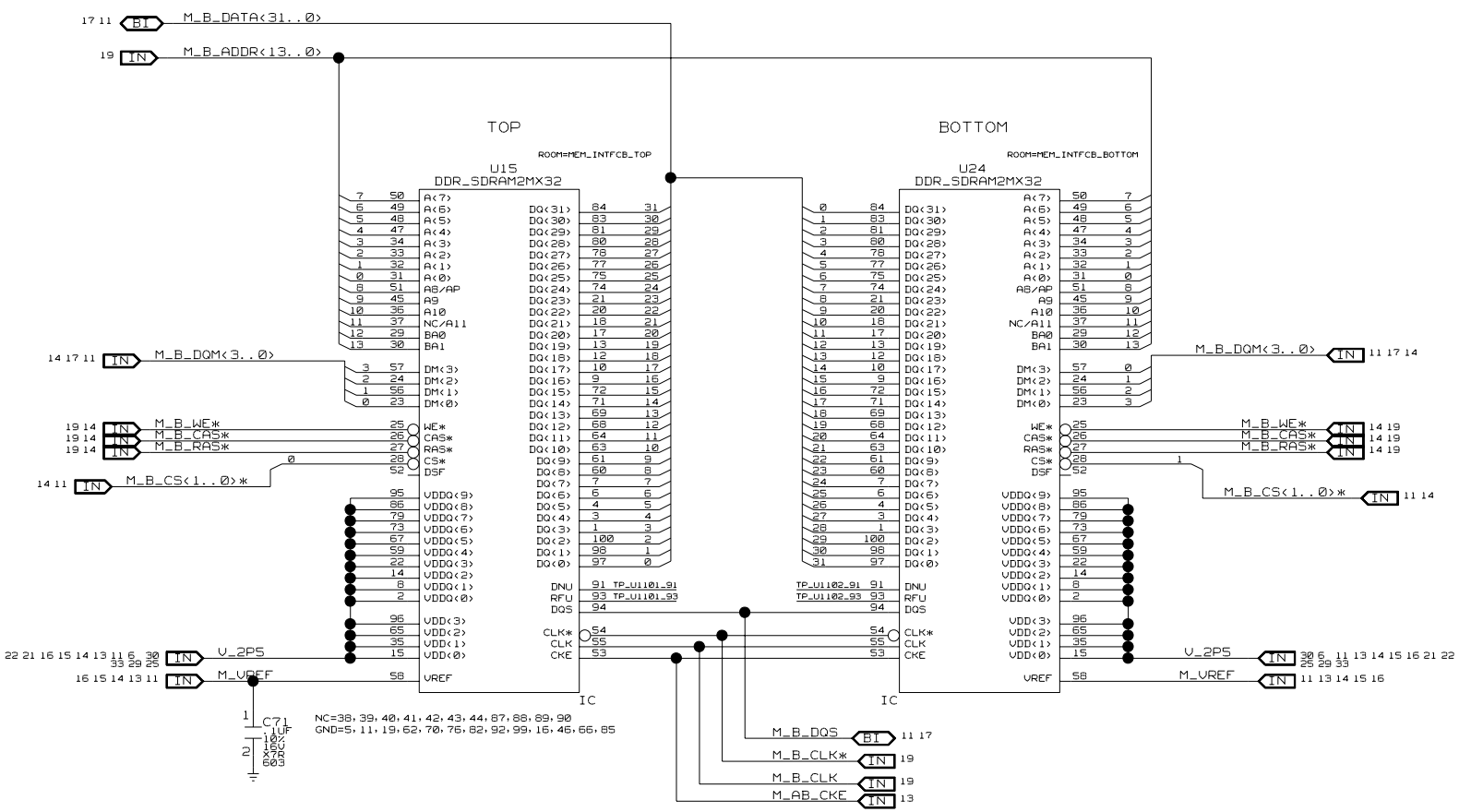
DRAWING
DVT.SCH_1.13
Fri Sep 01 07:31:20 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	13	0.13

CR-14

{FULL_ID=532-14-8168} {PAGE_INFO_ID=8168} {OWNED_BY=DE} {MODULE_ID=532-14-8168} {DONOR_ID=532-14-8168}

MEMORY INTERFACE PARTITION B



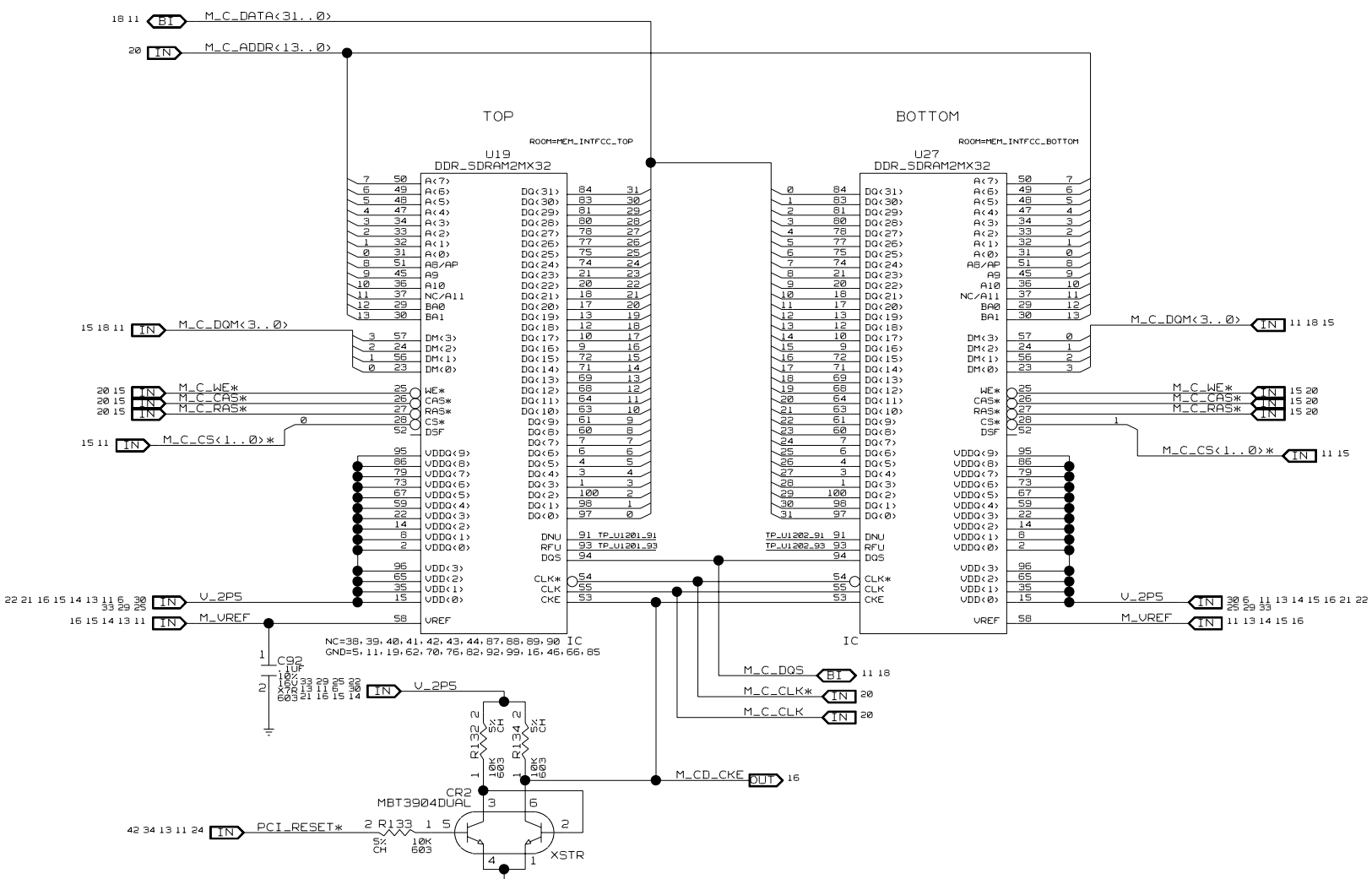
[PAGE_TITLE=DDR SDRAM (PARTITION B)]

DRAWING
DVT.SCH_1.14
Fri Sep 01 07:31:15 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	14	0.13

{DONOR_REV=} {DONOR_PROJ=} {PROJ_REV=0.13/page=14} {PROJ_NAME=DVT_A--532} {MODULE=NONE} {LAST_MAKEPROJ: 9/1/00 8:54:24 AM}

MEMORY INTERFACE PARTITION C

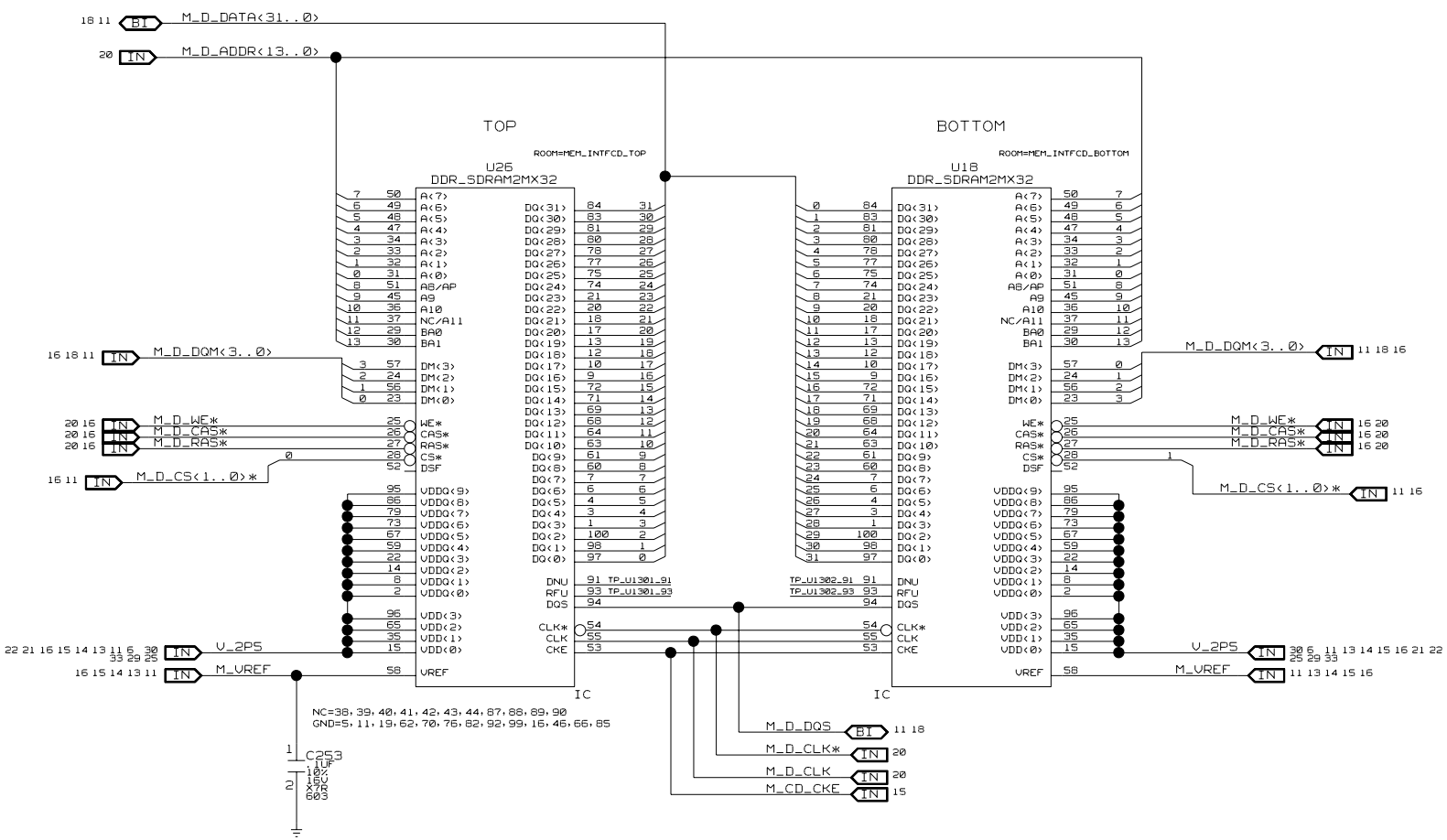


[PAGE_TITLE=DDR SDRAM (PARTITION C)]

DRAWING
DVT.SCH_1.15
Fri Sep 01 07:31:11 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	15	0.13

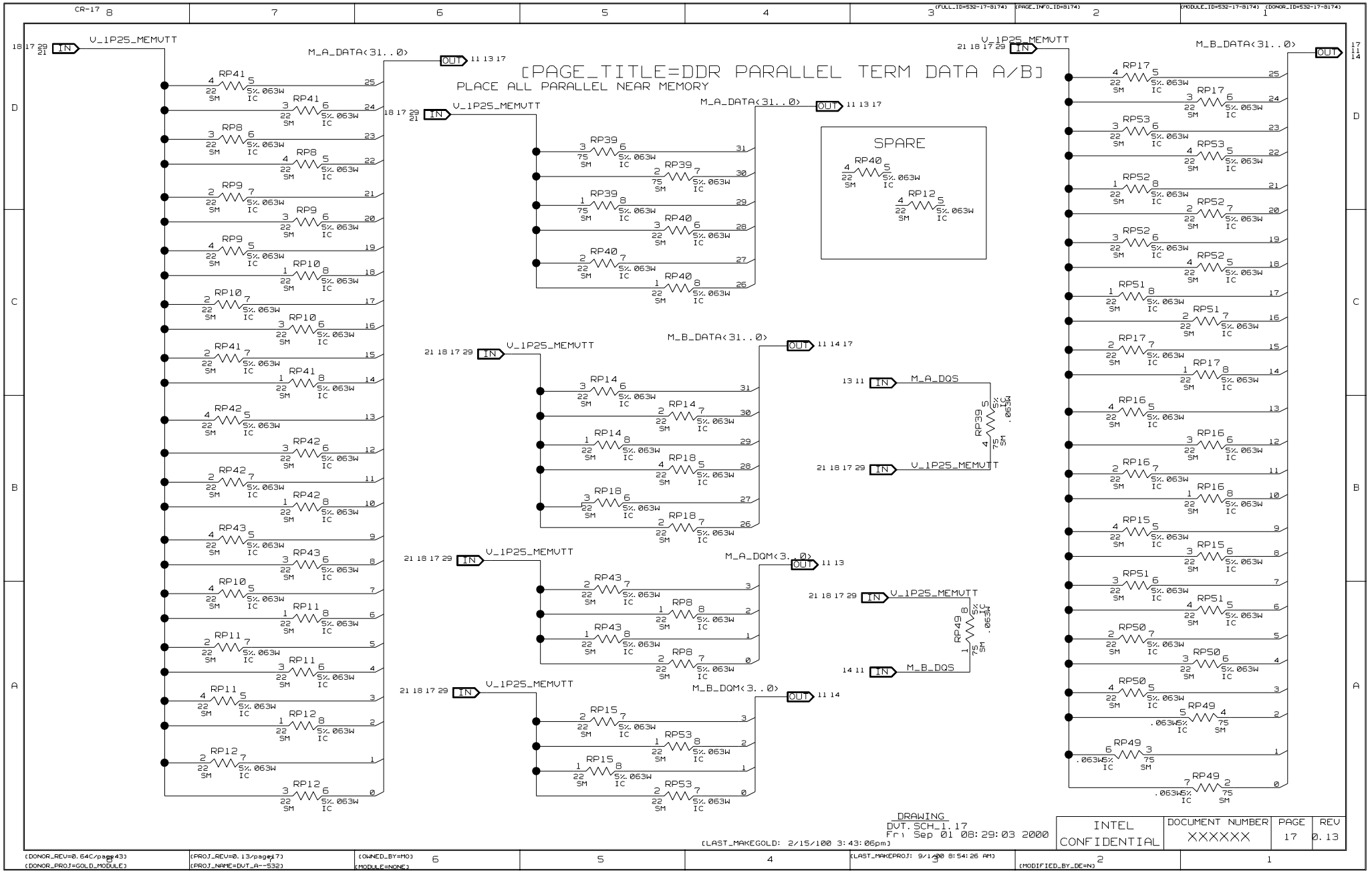
MEMORY INTERFACE PARTITION D

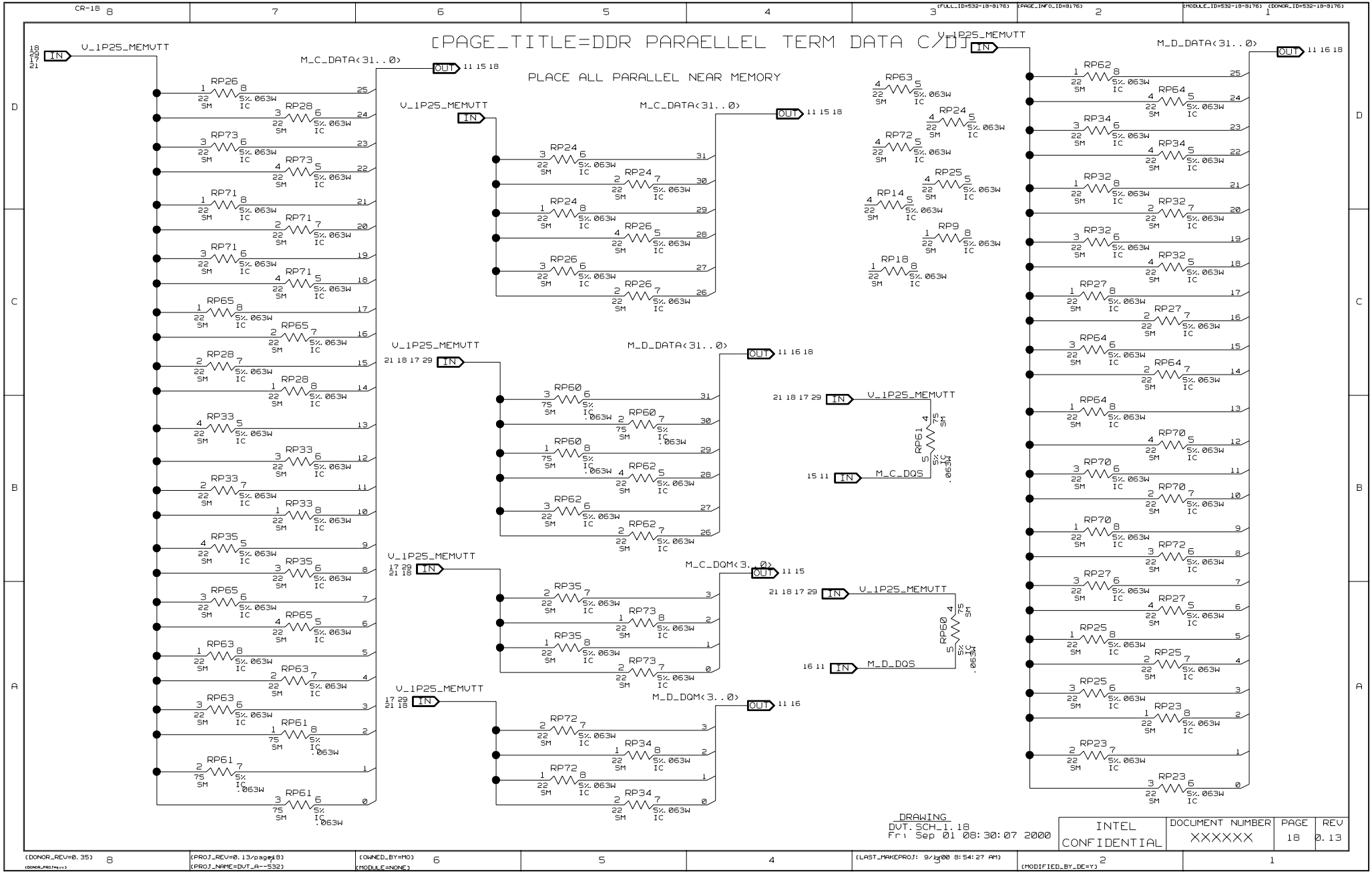


[PAGE_TITLE=DDR SDRAM (PARTITION D)]

DRAWING
DVT.SCH_1.16
Fri Sep 01 07:31:06 2000

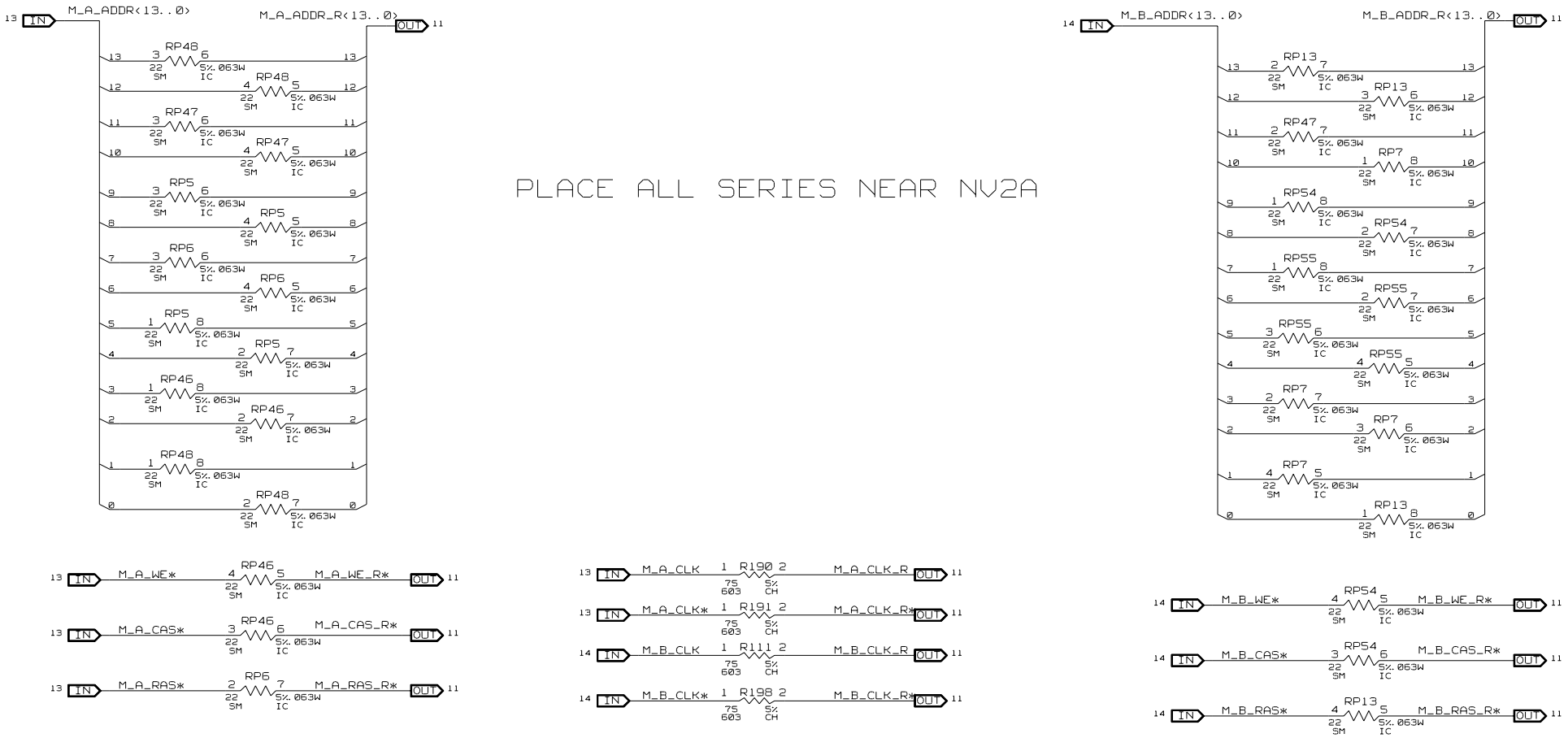
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	16	0.13


[PAGE_TITLE=DDR PARALLEL TERM DATA A/B]
PLACE ALL PARALLEL NEAR MEMORY
V_1P25_MEMVTT
M_A_DATA<31..0>
M_B_DATA<31..0>
M_A_DQM<3..0>
M_B_DQM<3..0>
M_A_DQS
M_B_DQS
SPARE
RP41
RP8
RP9
RP10
RP11
RP12
RP39
RP40
RP14
RP18
RP43
RP42
RP17
RP53
RP52
RP51
RP16
RP15
RP50
RP49
RP0
RP1
RP2
RP3
RP4
RP5
RP6
RP7
22 SM
75 SM
5% .063W IC
DRAWING
DVT.SCH_1.17
Fri Sep 01 08:29:03 2000
INTEL CONFIDENTIAL
DOCUMENT NUMBER XXXXXX
PAGE 17
REV 0.13


[PAGE_TITLE=DDR PARAELLEL TERM DATA C/D]
PLACE ALL PARALLEL NEAR MEMORY
V_1P25_MEMVTT
M_C_DATA<31..0>
M_D_DATA<31..0>
M_C_DQM<3..0>
M_D_DQM<3..0>
M_C_DQS
M_D_DQS
RP26
RP28
RP73
RP71
RP65
RP33
RP35
RP63
RP61
RP24
RP60
RP62
RP72
RP34
RP64
RP70
RP27
RP25
RP23
RP63
RP24
RP72
RP25
RP14
RP9
RP18
RP61
RP60
DRAWING
DUT.SCH_1.18
Fri Sep 01 08:30:07 2000
INTEL CONFIDENTIAL
DOCUMENT NUMBER
XXXXXX
PAGE
18
REV
0.13

CR-19

[FULL_ID=532-19-8178] [PAGE_INFO_ID=8178] [MODULE_ID=532-19-8178] [DONOR_ID=532-19-8178]



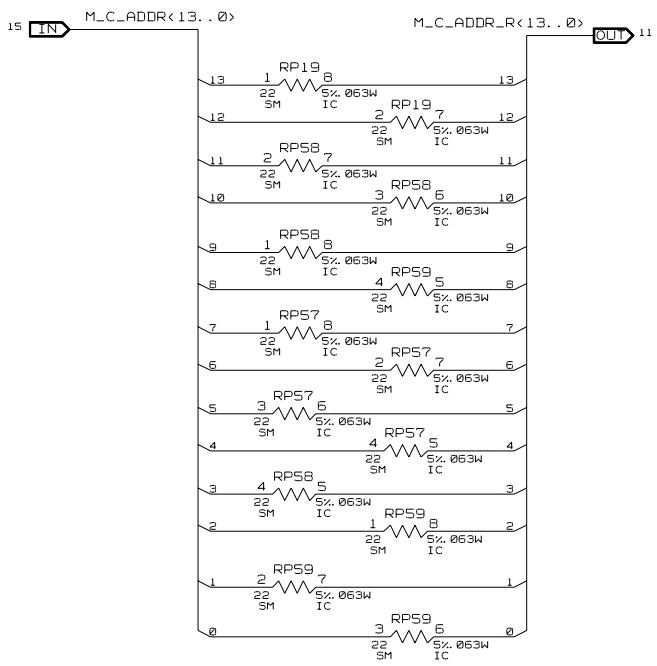
[PAGE_TITLE=DDR SERIES TERM ADDR A/B]

DRAWING
DVT.SCH_1.19
Fri Sep 01 07:30:52 2000

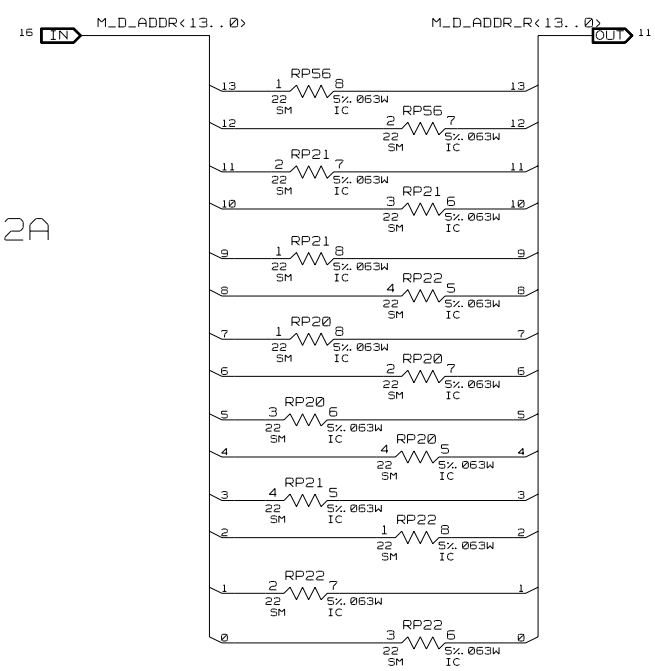
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	19	0.13

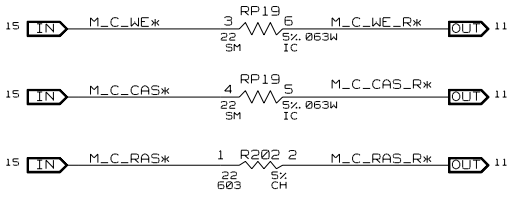
[MODULE=AUDIO] [SOLUTION=AUDIO/AUDIO] [MOD_PAGE=page43] [MOD_REV=0.64C] [LAST_MAKEGOLD: 2/15/100 3:43:06pm]

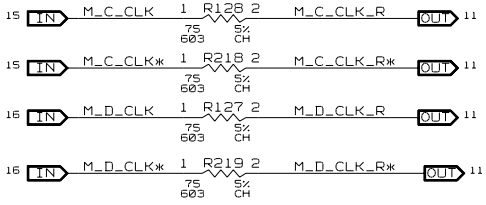
[DONOR_REV=0.64C/page43] [DONOR_PROJ=GOLD_MODULE] [PROJ_REV=0.13/page19] [PROJ_NAME=DVT_A--532] [OWNED_BY=MO] [LAST_MAKEPROJ: 9/1/00 8:54:27 AM] [MODIFIED_BY_DE=NJ]

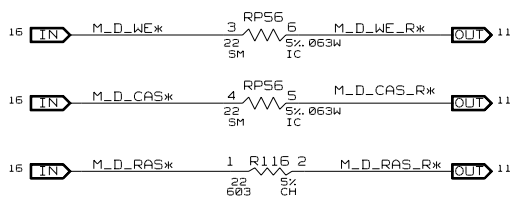


PLACE ALL SERIES NEAR NV2A





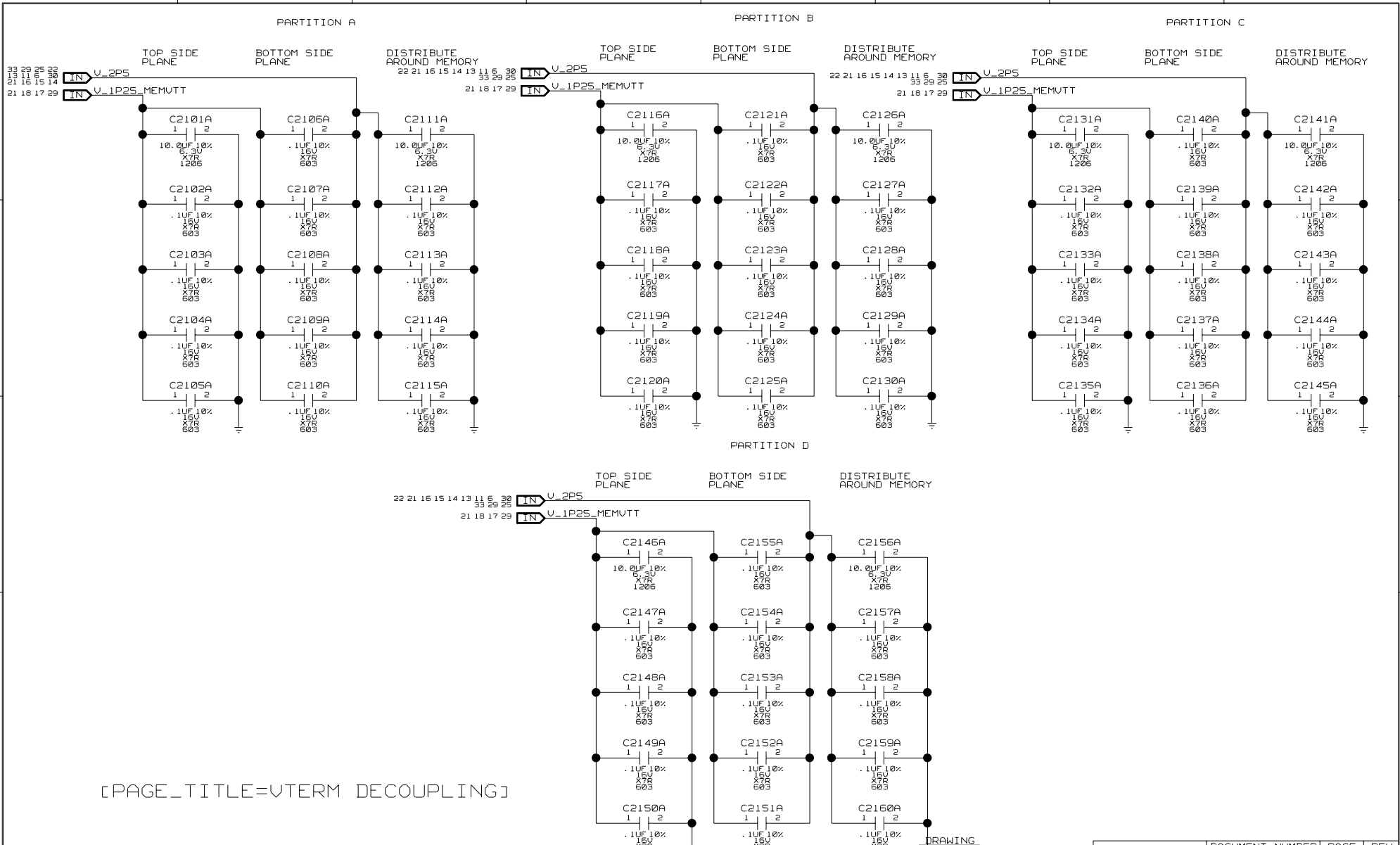




[PAGE_TITLE=DDR SERIES TERM ADDR C/D]

DRAWING
DUT.SCH_1.20
Fri Sep 01 07:30:47 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	20	0.13

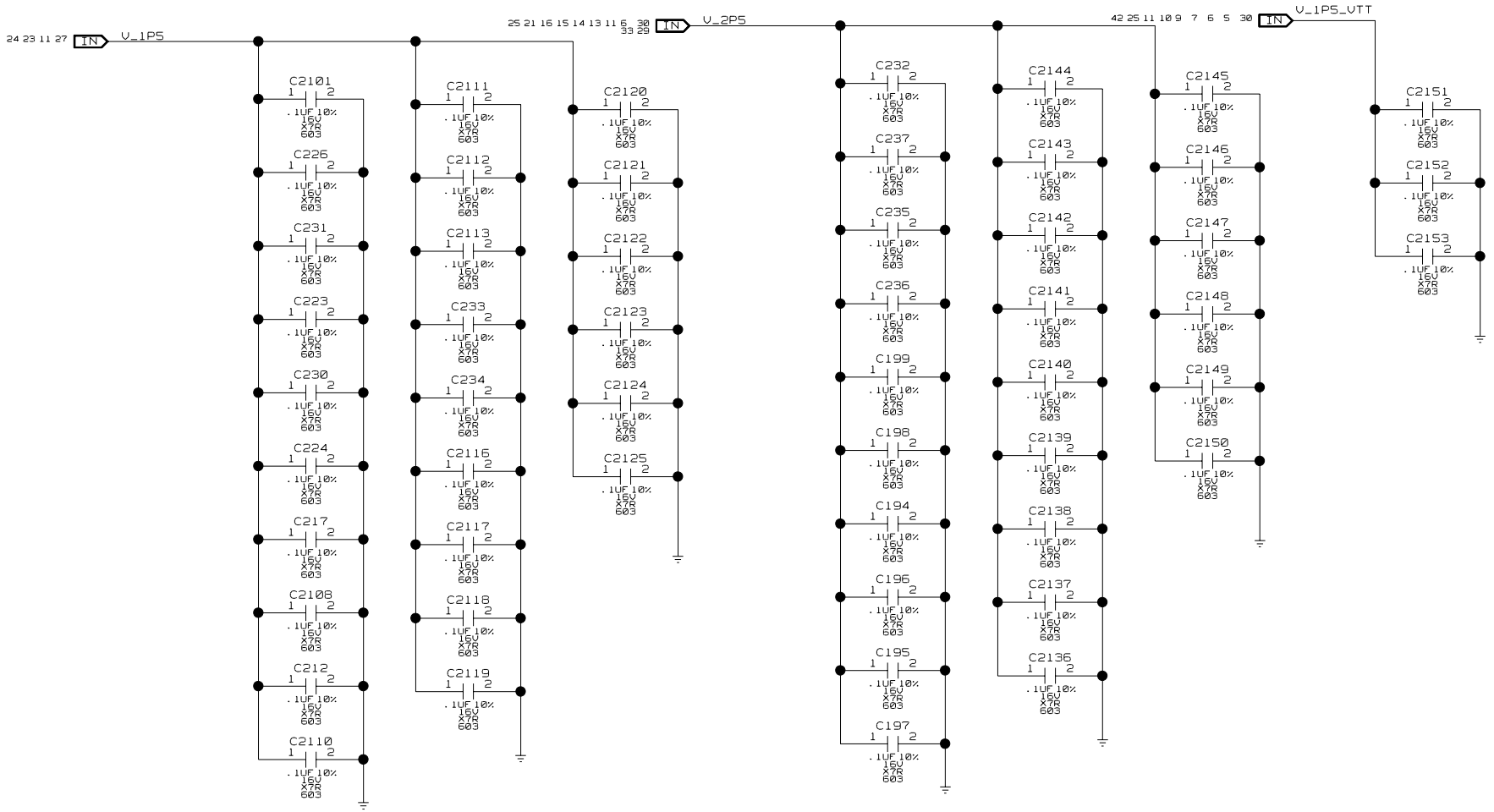


[PAGE_TITLE=VTERM DECOUPLING]

DRAWING
DVT.SCH_1.21
Fri Sep 1 08:19:02 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	21	

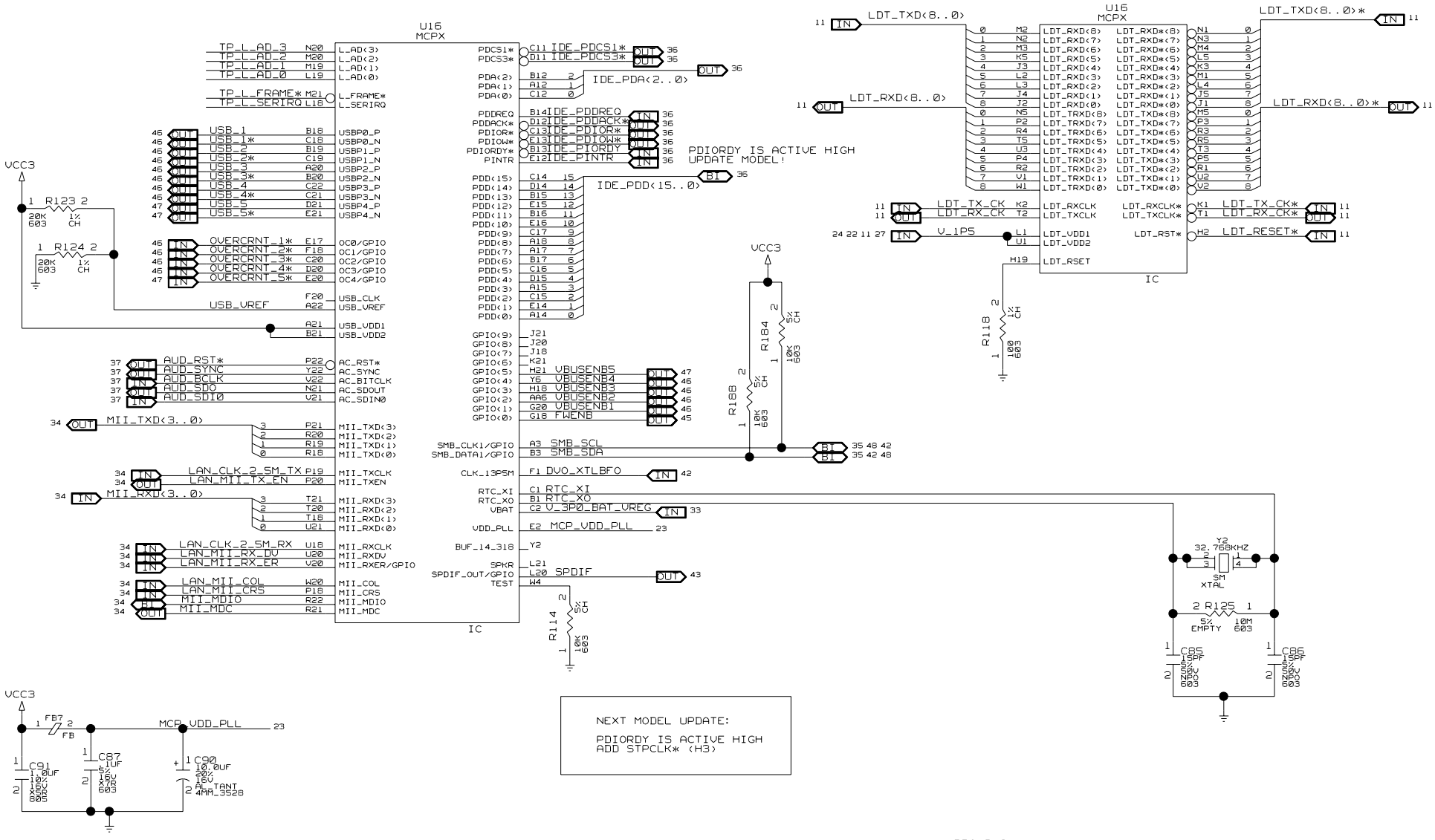
NV2A DECOUPLING



[PAGE_TITLE=NV2A DECOUPLING]

DRAWING
DVT.SCH_1.22
Fri Sep 01 07:30:38 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	22	0.13

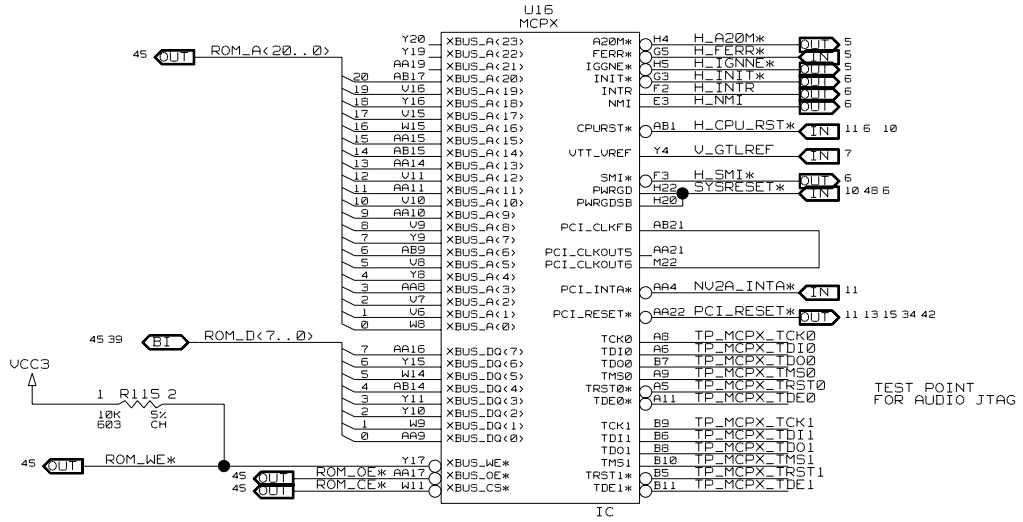


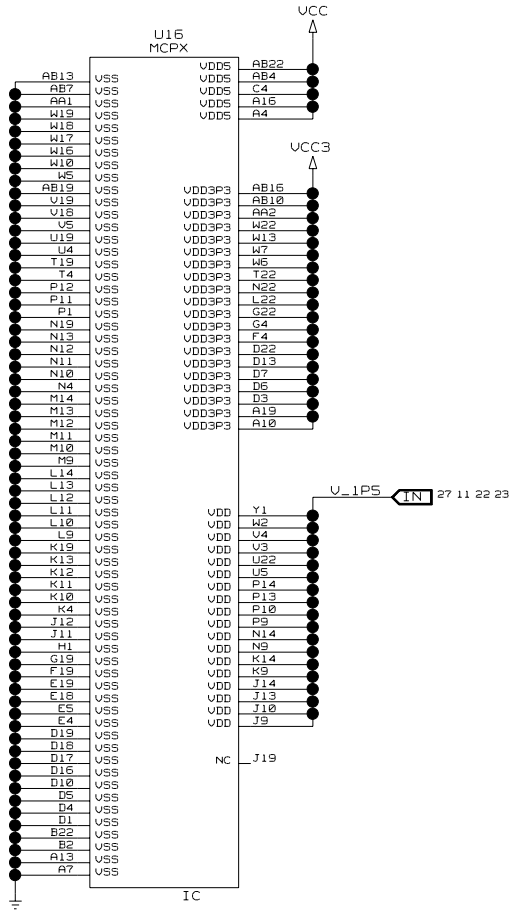
[PAGE_TITLE=MCPX 1 OF 2]

DRAWING
DVT.SCH_1.23
Fri Sep 01 07:30:33 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	23	0.13

[DONOR_REV=]
[DONOR_PROJ=]
[PROJ_REV=0.13/page=23]
[PROJ_NAME=DVT_A--532]
[MODULE=NONE]
[LAST_MAKEPROJ: 9/1/00 8:54:29 AM]
[FULL_ID=532-22-8184] [PAGE_INFO_ID=8184] [OWNED_BY=DE] [MODULE_ID=532-22-8184] [DONOR_ID=532-22-8184]
CR-23

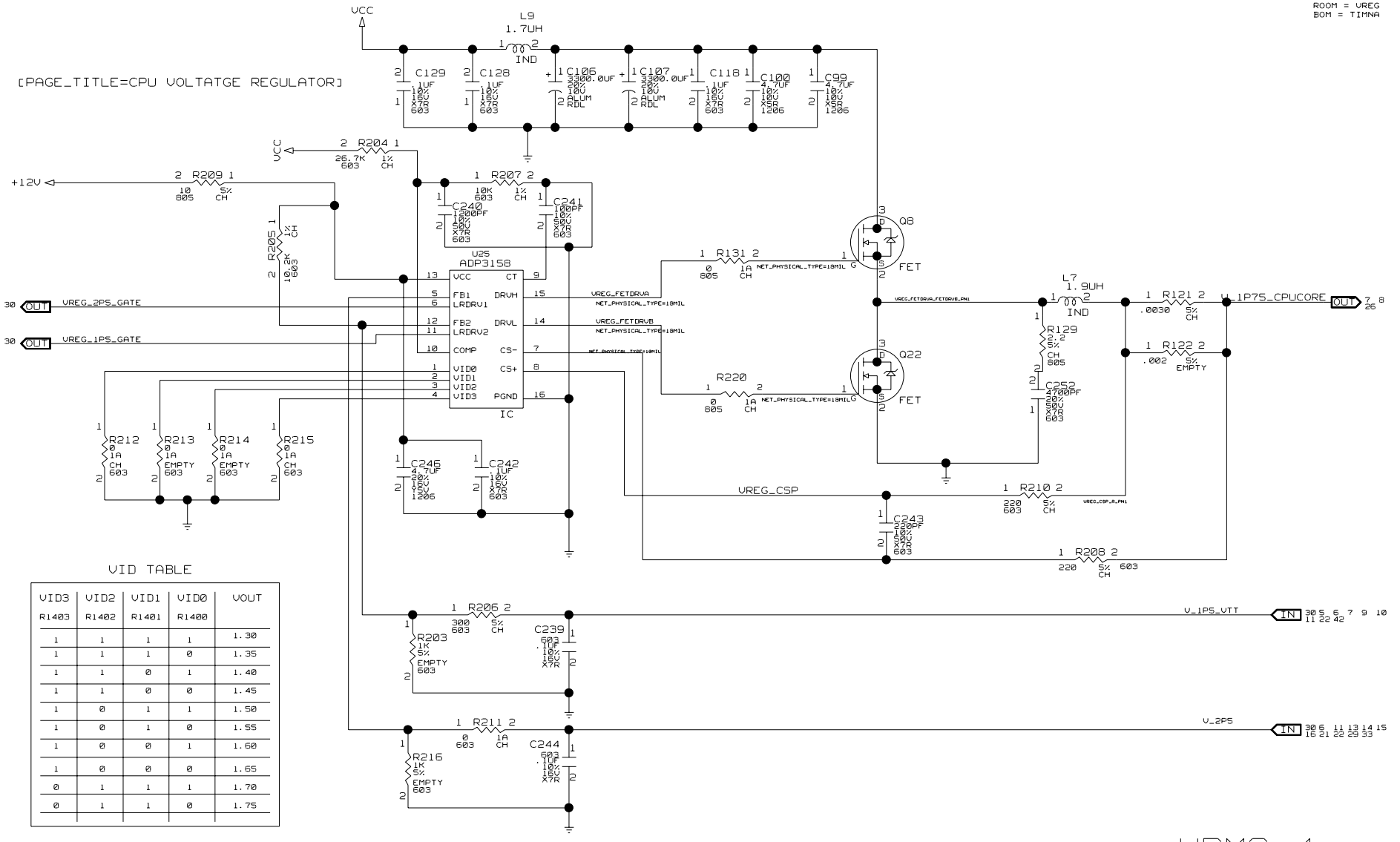




[PAGE_TITLE=MCPX 2 OF 2]

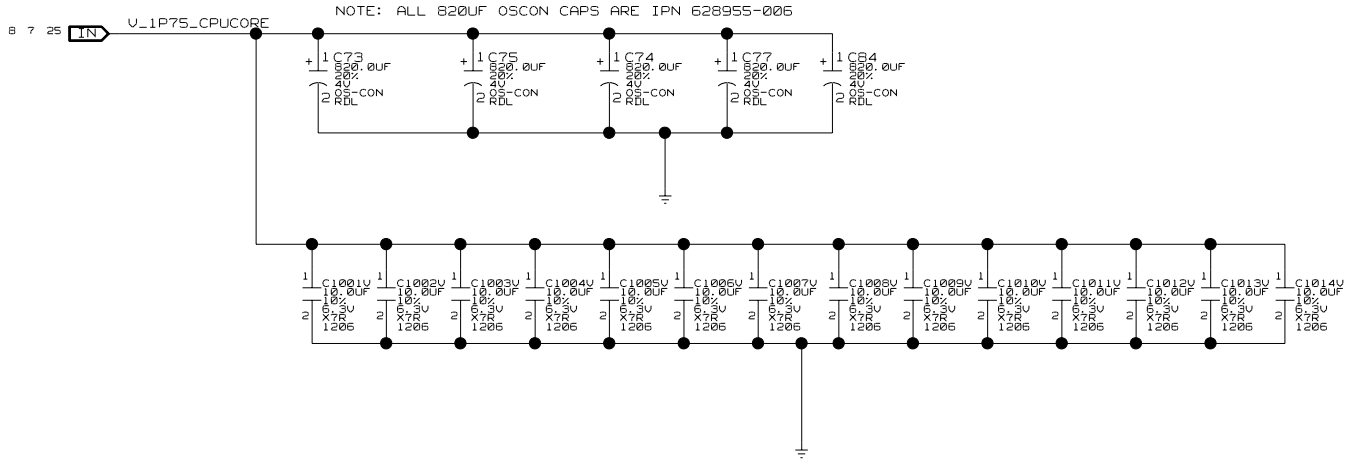
DRAWING
DVT.SCH_1.24
Fri Sep 1 08:19:02 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	24	


LAST USED:
R814V
L802V
C813V
U801V
CR801V
[PAGE_TITLE=CPU VOLTATGE REGULATOR]
ROOM = VREG
BOM = TIMNA
VCC
L9
1.7UH
IND
C129
C128
C106
3300.0UF
C107
3300.0UF
C118
C100
4.7UF
C99
4.7UF
R204
26.7K
R209
10
R207
10K
C240
C241
R205
10.2K
U25
ADP3158
VCC
CT
FB1
DRVH
LRDRV1
FB2
DRVL
LRDRV2
COMP
CS-
VID0
CS+
VID1
VID2
VID3
PGND
IC
VREG_2P5_GATE
VREG_1P5_GATE
VREG_FETDRVA
VREG_FETDRVB
R131
R220
QB
Q22
FET
L7
1.9UH
R129
C252
4700PF
R121
.0030
R122
.002
1P75_CPUCORE
VREG_CSP
R210
220
C243
R208
R212
R213
R214
R215
C246
4.7UF
C242
R206
300
R203
1K
C239
V_1P5_VTT
R211
R216
C244
V_2P5
VID TABLE
VID3 R1403
VID2 R1402
VID1 R1401
VID0 R1400
VOUT
1.30
1.35
1.40
1.45
1.50
1.55
1.60
1.65
1.70
1.75
0= RESISTOR IS STUFFED.
1= RESISTOR IS UNSTUFFED.
VRM8.4
DRAWING
DVT.SCH_1.25
Fri Sep 01 07:30:24 2000
INTEL CONFIDENTIAL
DOCUMENT NUMBER
XXXXXX
PAGE
25
REV
0.13
[MODULE=VREG]
[SOLUTION=REG_CPU/CORE_REG]
[MOD_PAGE=page8]
[MOD_REV=0.04C]
[LAST_MAKEGOLD: 3/15/100 5:04:08pm]
[DONOR_REV=0.04C/page8]
[DONOR_PROJ=GOLD_MODULE]
[PROJ_REV=0.13/page25]
[PROJ_NAME=DVT_A--532]
[OWNED_BY=MO]
[LAST_MAKEPROJ: 9/1/00 8:54:30 AM]
[MODIFIED_BY_DE=NJ]

LAST USED
C1020V

ROOM= = VREG
BOM = TIMNA



OUTPUT FILTER

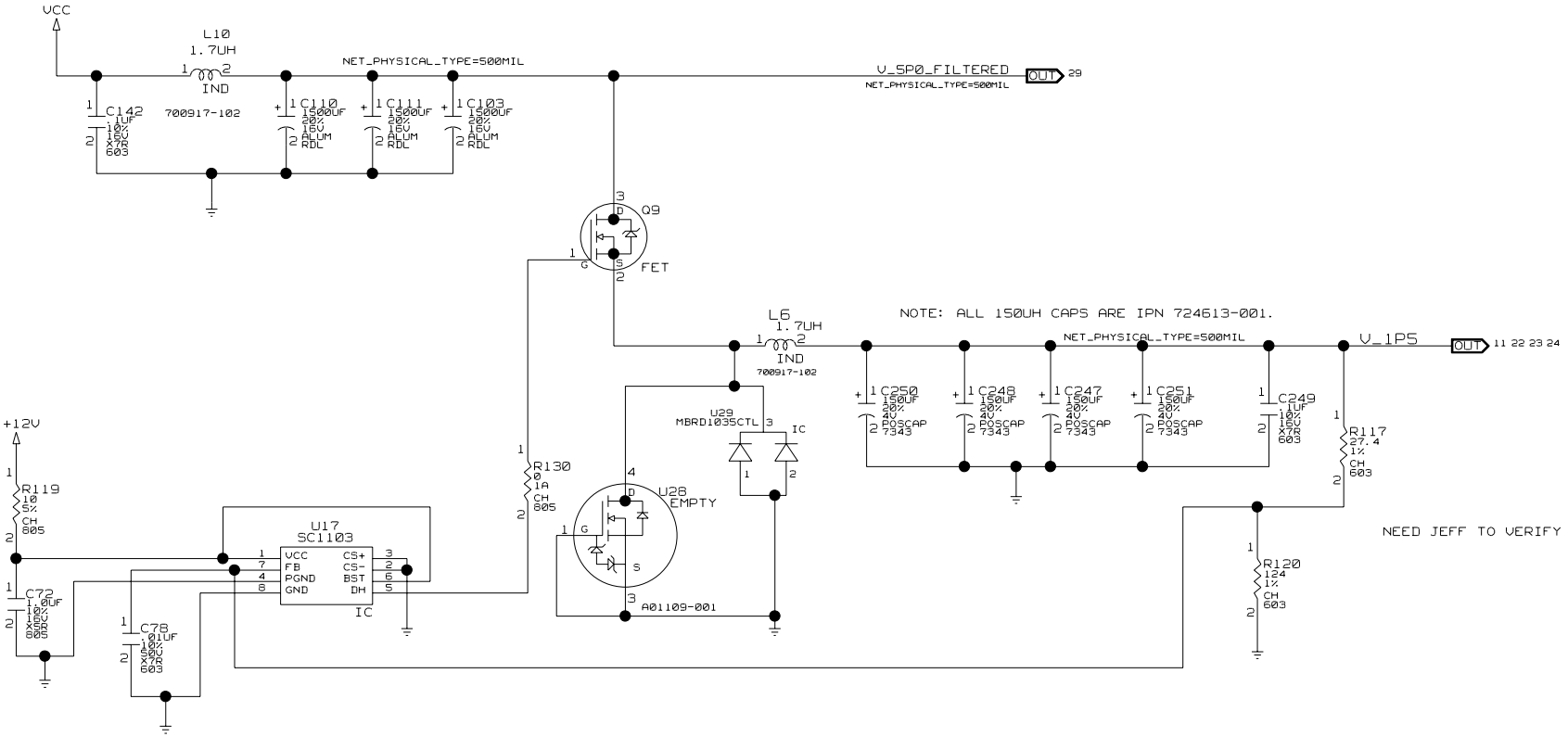
[PAGE_TITLE=CPU VREG OUTPUT FILTER]

DRAWING
DVT.SCH_1.26
Fri Sep 01 07:30:20 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	26	0.13

[MODULE=VREG] [SOLUTION=REG_CPU/CORE_REG] [MOD_PAGE=page10] [MOD_REV=0.04C]
[PAGE_TITLE=NO_TITLE]
[LAST_MAKEGOLD: 3/15/100 5:02:46pm]

[DONOR_REV=0.04C/page10]
[DONOR_PROJ=GOLD_MODULE]
[PROJ_REV=0.13/page26]
[PROJ_NAME=DVT_A--532]
[OWNED_BY=MO]
[LAST_MAKEPROJ: 9/1/00 8:54:31 AM]
[MODIFIED_BY_DE=NJ]



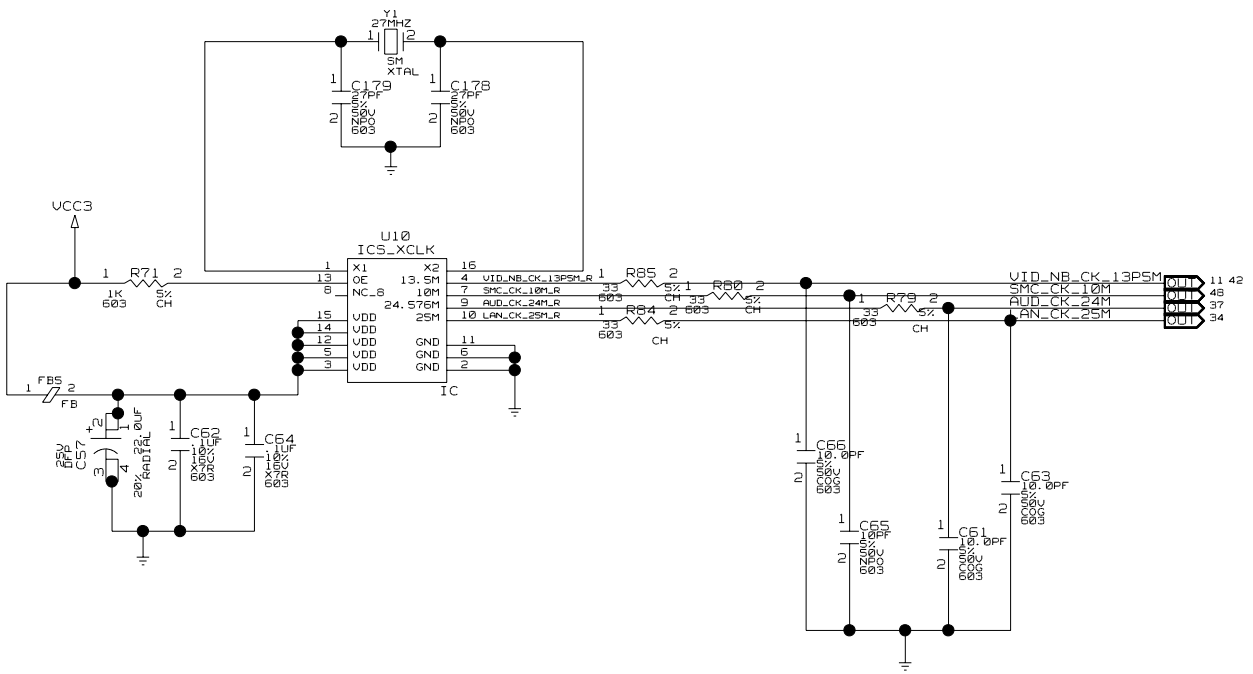
1.5V SWITCHING REGULATOR

[PAGE_TITLE=1.5V SWITCHING REGULATOR]

DRAWING
DVT.SCH_1.27
Fri Sep 01 07:30:15 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	27	0.13

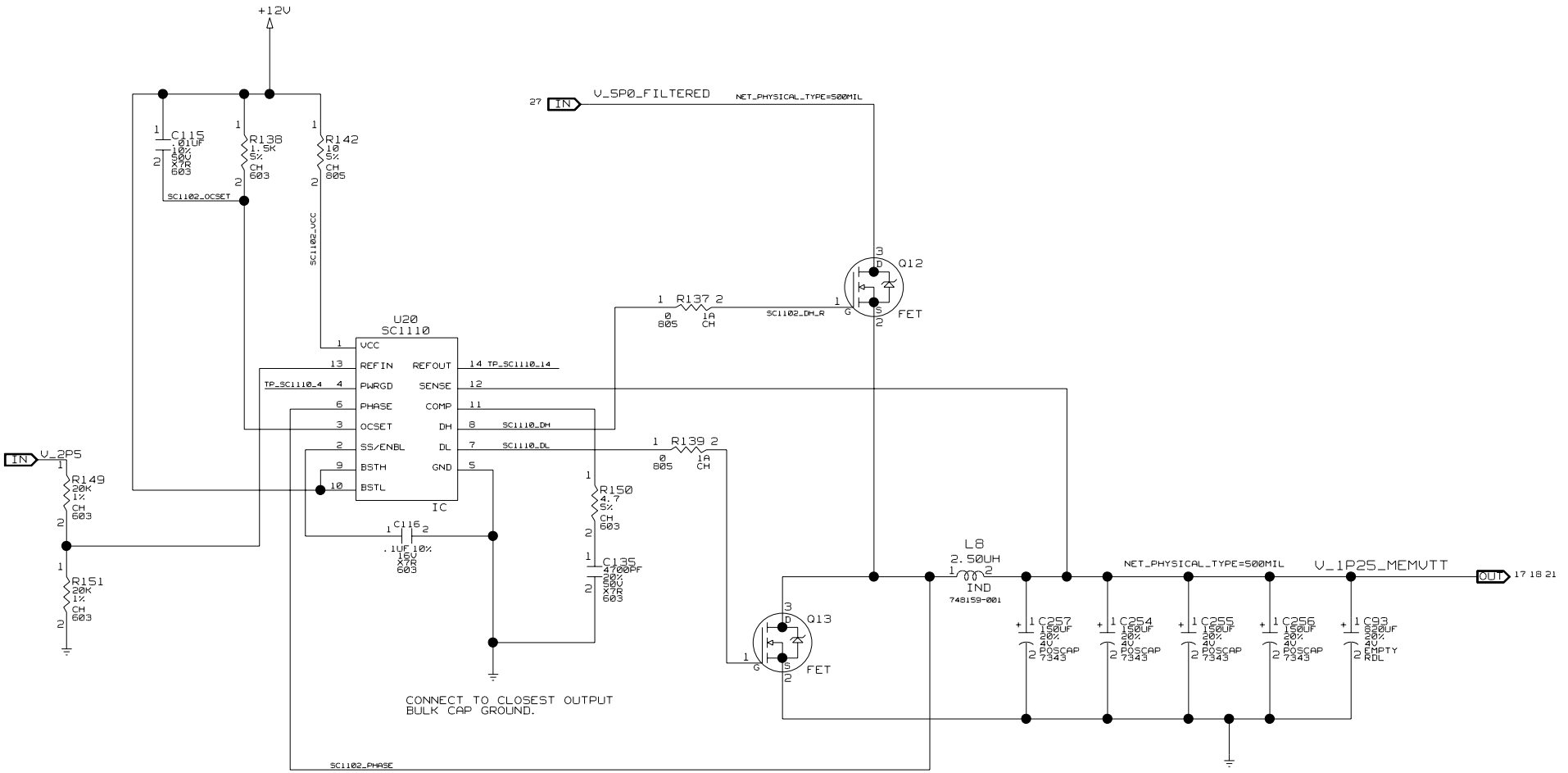
[DONOR_REV=]
[DONOR_PROJ=]
[PROJ_REV=0.13/page=27]
[PROJ_NAME=DVT_A--532]
[MODULE=NONE]
[LAST_MAKEPROJ: 9/1/00 8:54:31 AM]
[FULL_ID=532-25-8190] [PAGE_INFO_ID=8190] [OWNED_BY=DE] [MODULE_ID=532-25-8190] [DONOR_ID=532-25-8190]
CR-27



[PAGE_TITLE=CLOCK GENERATOR]

DRAWING
DVT.SCH_1.28
Fri Sep 01 07:30:10 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	28	0.13



NOTE: ALL 150UH CAPS ARE IPN 724613-001.

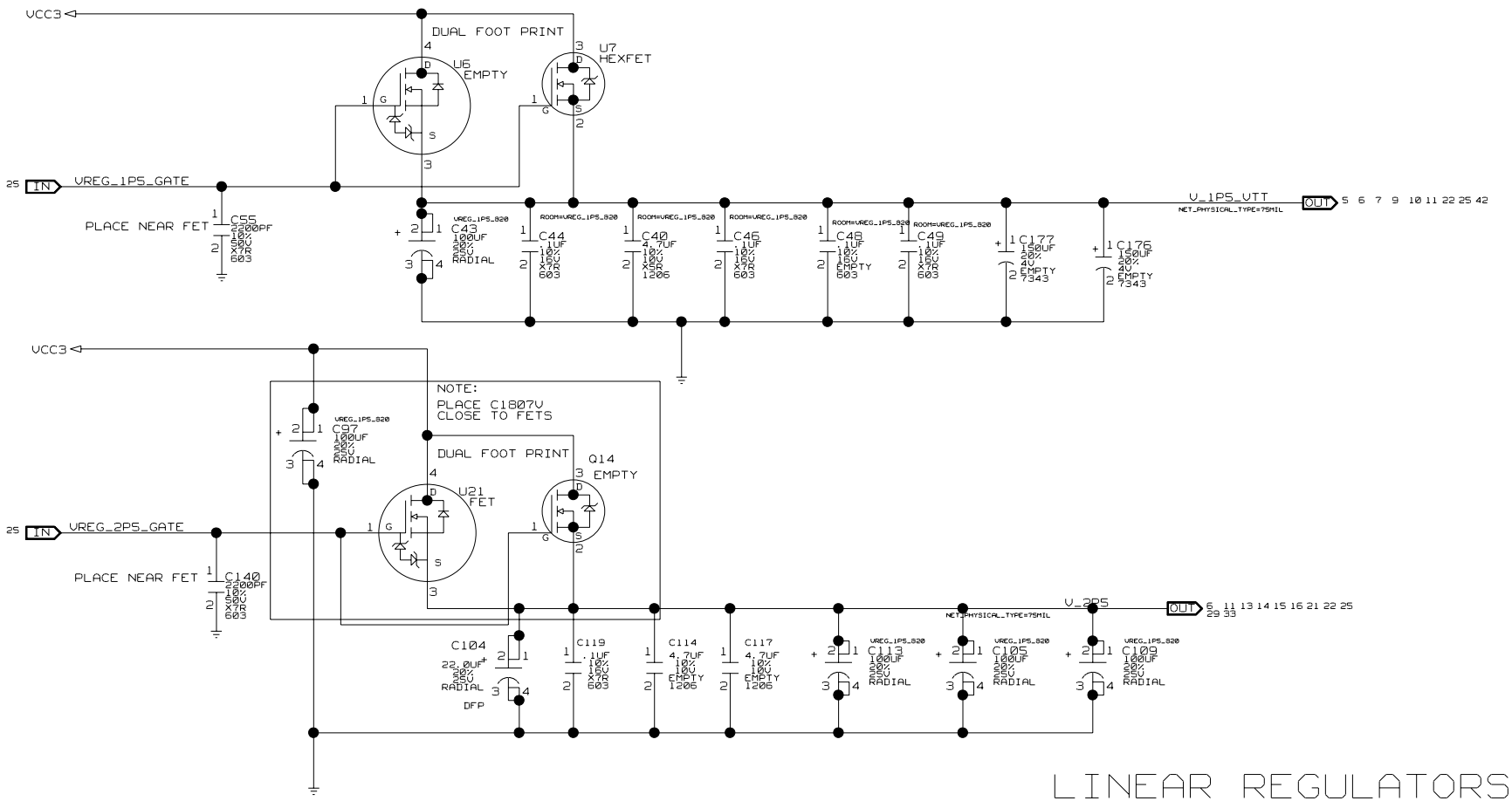
1.25V SWITCHING REGULATOR

[PAGE_TITLE=1.25V SWITCHING REGULATOR]

DRAWING
DVT.SCH_1.29
Fri Sep 01 07:30:06 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	29	0.13

LAST USED
Q1804V
C1810V
HS1810V



LINEAR REGULATORS (1.5V/2.5V)

[PAGE_TITLE=LINEAR_REGULATORS_1.5_2.5]

DRAWING
DVT.SCH_1.30
Fri Sep 01 07:30:01 2000

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	XXXXXX	30	0.13