MCP-1™

Media Communication Processor (South Bridge)

PRELIMINARY CONFIDENTIAL INFORMATION

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1.0 Revision History

Release	Version	Date	Description
-xxx	0.11	July 15, 2000	Initial release.
-xxx	0.12	July 18, 2000	Ball out updates (PRDY# & LDT_RST#)
-xxx	0.13	July 22, 2000	Ball out update (BUF_24M); Included AC/DC Info
-xxx	0.14	August 6, 2000	Updates (i.e. ROM Table) – Typo Cleanups
-xxx	0.15	August 15, 2000	Fix XBUS_DQ0 and XBUS_DQ1 swap in Section 8.5. (Was correct elsewhere.)

2.0 Overview

The Media Communications Processor - 1 (MCP-1) is the next generation of highly integrated, high performance, low cost PC 2001 compliant Core Logic Controllers (South Bridge) that support both AMD™ and Intel® processor bridge functionality.

The MCP-1 implements the fastest dedicated North – South Link (LDT™ interface) running at 800MB/sec to communicate with the CRUSH 11/12™ (North Bridge with integrated Graphics Processing Unit). This ensures that the bandwidth required by current Peripheral devices; such as ATA-100, USB, Fast Ethernet, and Audio/Modem devices, as well as any future devices, will be available and not impact bus performance.

The MCP-1 integrates dual fast IDE controllers. It supports the standard PIO and DMA mode operations as well as the UltraDMA-100/66/33 (ATA-100/66/33) standard for a maximum data transfer rate of 100MB/sec per channel. It provides separate independent data paths for the two IDE channels that significantly improve performance. The two independent channels can be configured to the standard primary and secondary channels that allow up to 4 devices to be connected; such as HDD, DVD, R/W CD, etc. All IDE signals are 5V tolerant.

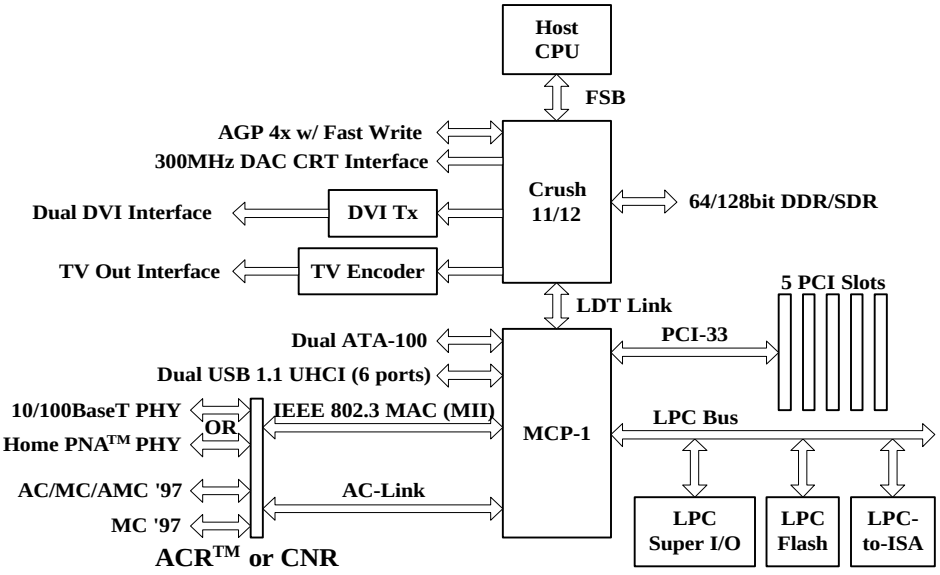
The MCP-1 integrates a total communications solution that supports both the Advanced Communication Riser (ACR™) and Communication and Networking Riser (CNR) Specifications. It's IEEE 802.3 compatible MAC (MII) supports 10/100 BaseT Ethernet/Fast Ethernet PHYs for Office Networking. It can also support HomePNA™ 1.0/2.0 compatible PHYs for Home Networking. It integrates dual USB 1.1 OHCI controllers that can support up to 6 ports to communicate to the USB devices. The USB ports can be configured for 3/3 or 2/4. It integrates an AC '97 2.1 Compliant Interface (AC-Link) to communicate to Audio and Modem CODECs. Two independent CODECs can be supported with the AC-Link. An audio (AC), modem (MC), audio/modem (AMC) CODEC, or both an AC and a MC can be supported. Microphone input and left and right audio channels are supported for a high quality two speaker audio solution.

The MCP-1 integrates an LPC 1.0 compatible interface and AT Legacy functionality support. This includes dual-8259 PIC, an 82093 compatible I/O APIC, dual-8237 DMA controllers, and an 8254 programmable interval timer. It also includes a MC146818A/DS12887 compatible RTC with 256byte battery backed-up RAM. The LPC interface can be used to connect to Super I/O, Flash, and LPC-to-ISA Bridge devices.

The MCP-1 integrates a Fast PCI-to-PCI bridge with an external PCI bus behind a PCI-to-PCI bridge that is PCI rev 2.2 compliant running at 33MHz. It includes an arbiter that allows support of up to 5 external PCI slots. All PCI signals are 5V tolerant.

The MCP-1 integrates a Clock Synthesizer to generate all the necessary internal/external clock frequencies with spread spectrum capabilities.

The MCP-1 supports both the ACPI 1.0 and PCI PM 1.1 Specifications and the IAPC for power management of all necessary internal blocks and external peripherals.



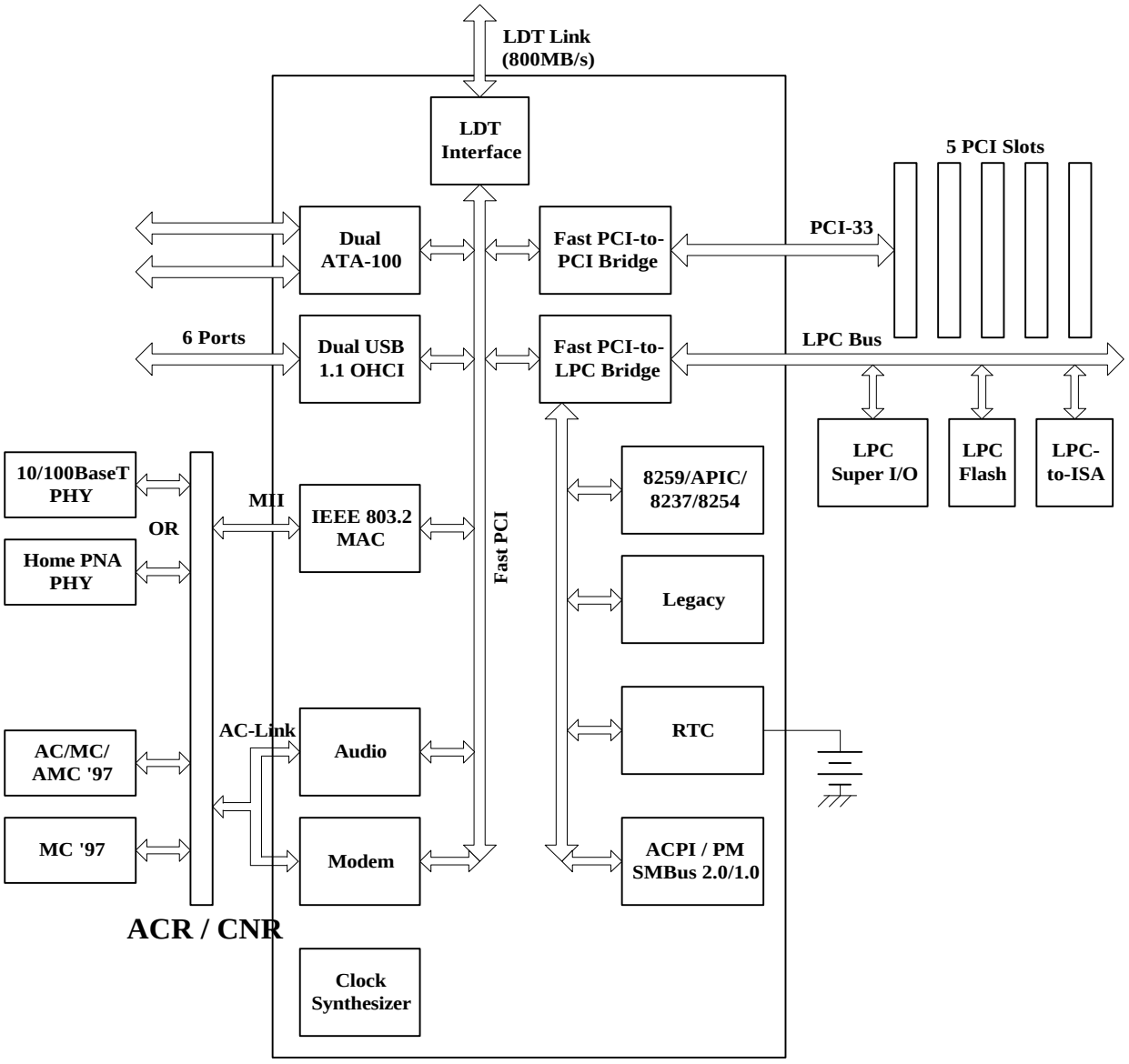
3.0 Feature List

- LDT Link to communicate with the CRUSH 11/12
  - High Speed (800MB/sec Peak – Scalable), Differential, Bi-Directional, and Low Pin Count
  - Isochronous and Asynchronous Queue
    - Pipeline Reads and Writes
- Dual Concurrent Ultra DMA IDE Controllers
  - Industry Standard PCI Bus Master IDE Register Set
  - Separate Independent IDE Connections for Primary and Secondary Interfaces (5V Tolerant)
    - Each Interface supports two devices for a total of four devices
    - Independent Transmit and Receive FIFOs for maximum performance
  - Supports standard PIO Mode 0, 1, 2, 3, and 4
  - Supports standard DMA Mode 0, 1, and 2
  - Supports Ultra DMA Mode 0, 1, 2, 3, 4, and 5 (Ultra DMA-100/66/33)
- Advanced Communication Riser (ACR) and Communication and Networking Riser (CNR) Interface
  - Dual USB 1.1 OHCI Controller that supports 6 Ports
    - Configurable as 3/3 or 2/4
    - Supports Full Speed (12Mb/sec) and Low Speed (1.5Mb/sec) per Port
    - Allows USB Concurrency
    - Per Port Over-Current Protection
  - IEEE 802.3 MAC (Media Access Control)
    - Supports 10/100 BaseT Ethernet/Fast Ethernet or HomePNA 1.0/2.0 PHYs
    - Carrier Sense Multiple Access / Collision Detect (CSMA / CD)
      - Compliant with IEEE 802.3 and 802.3u (MII)
  - AC ’97 2.1 Compliant Interface
    - AC-Link – Supports up to two CODECs
      - Supports AC/MC/AMC ’97 CODEC as primary
      - Supports MC ’97 CODEC as secondary
    - Both 48KHz Fixed and Variable Audio CODEC Support
    - 16-bit or 24-bit Stereo, Quad or 6-channel Output
    - 16-bit Stereo Input Streams
    - Supports Input, Output, and GPIO Channels for Host Based Modems
    - Separate Independent Functions for Audio and Modem
    - Flexible Six Independent DMA Controllers
      - For Audio In, Audio Out, SPDIF Out, Modem In, Modem Out, and MIC In
    - S/PDIF Output
      - Stereo or AC-3 Output
      - 16-bit or 24-bit PCM Support
      - 48KHz Support Only
- Internal Fast PCI-to-PCI Bridge – version 2.2 compliant (5V Tolerant)
  - Supports up to 5 external PCI slots at 33MHz
    - Supports 5 Bus Master Arbitration and PCI Interrupts
  - PCI Master and Slave Interfaces
  - Supports both Master and Slave Initiated Terminations
  - Bi-Directional Write Posting Support for Concurrency
  - Read Ahead – MRL (memory read line) and MRM (memory read multiple) Support

- Internal Fast PCI-to-LPC Bridge
  - Subtractive Decode
  - Can be connected to external Super I/O, Flash BIOS, and LPC-to-ISA Bridge chips
  - Supports LPC DMA and Mastering
    - Supports 2 DMA/Masters
  - Serial Interrupt Protocol Support
  - Three Programmable Positive Decode Regions
- Integrated dual-8259, 82093 compatible I/O APIC, dual-8237, 8254 for Legacy AT Support
  - Interrupt Control
    - Dual 8259 supports 15 Interrupts
    - I/O APIC supports 24 Interrupts
    - PCI Interrupt Routing and Masking
    - Independent Edge/level Triggered Interrupts
    - Interrupt Sharing for all Internal Devices
  - DMA Control
    - Dual 8237 supports 7 Independently Programmable Channels
    - Standard and Extended Page Registers to allow 32-bit Addressing
  - Timer Counter
    - Based on 14.31818MHz Clock or Crystal
  - All AT Compatible Registers
- Integrated MC146818A/DS12887 compatible RTC
  - 256byte Battery Backed CMOS RAM
  - ACPI Wake-up event for Day of Month and Time of Day
  - Century Rollover, Leap Year, and Daylight Savings Compensation Support
- Dual System Management Bus (SMBus) 2.0 Interface (5V Tolerant)
  - PEC and ARP Support
  - SMBus Host and Slave Support
  - SMBus Alert Support
- DDC Interface (5V Tolerant)
- Power Management
  - IAPC – Instantly Available PC
  - ACPI 2.0 and PCI PM 1.1 Support
  - PME# Detection
  - SMI# Generation
  - Clock Generator Control
  - CPU Power State Control
  - 33 Multiplexed and Individually Configurable GPIO pins
  - Thermal Event Detection (Alarm)
  - Suspend to RAM and Disk Support
- System Management
  - WfM – Wired for Management and WoL – Wake on LAN
  - TCO Features
    - TCO Timer, Processor Presence Detection, Intruder Detection,
    - CPU Clock Frequency Control, Function Disable, Legacy Disable
- Integrated Clock Synthesizer
  - MCP-1, LDT, PCI, IDE, and USB Clocks
  - Spread Spectrum Capability

The MCP-1 is in a 376 PBGA 0.15u process 1.2V core with a 3.3V interface

3.1 MCP-1 Block Diagram



4.0 Signal List

5.0 Signal Definitions

The '#' symbol at the end of a signal name indicates that the active, or asserted state, occurs when the signal is at a LOW voltage level. When the '#' is not present after the signal name, the signal is asserted at a HIGH voltage level.

The following notations are used to describe the signal types:

I	Input
O	Output
OD	Open Drain Output
I/O	Bi-directional Input / Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
DIFF I/O	Differential Input / Output
A	Analog
P	Power

5.1 LDT (North – South) Link Interface

Signal	I/O	Definition
LDT_RSET	A	LDT Link Current Reference. This is the current reference for the integrated LDT drivers and receivers.
LDT_RST#	I	LDT Link Reset. This signal will reset the LDT Link.
LDT_RXCK	DIFF IN	LDT Link Positive Differential Receive Clock. This signal is the positive signal of a differential pair used as the timing reference for LDT_RXD[8:0].
LDT_RXCK#	DIFF IN	LDT Link Negative Differential Receive Clock. This signal is the negative signal of a differential pair used as the timing reference for LDT_RXD[8:0].
LDT_RXD[8:0]	DIFF IN	LDT Link Positive Differential Receive Data[8:0]. These signals are the positive signals of a differential pair used to receive the high speed 8-bits of information from the CRUSH 11/12 (North Bridge).
LDT_RXD[8:0]#	DIFF IN	LDT Link Negative Differential Receive Data[8:0]. These signals are the negative signals of a differential pair used to receive the high speed 8-bits of information from the CRUSH 11/12 (North Bridge).
LDT_TXCK	DIFF OUT	LDT Link Positive Differential Transmit Clock. This signal is the positive signal of a differential pair used as the timing reference for LDT_TXD[8:0].
LDT_TXCK#	DIFF OUT	LDT Link Negative Differential Transmit Clock. This signal is the negative signal of a differential pair used as the timing reference for LDT_TXD[8:0].
LDT_TXD[8:0]	DIFF OUT	LDT Link Positive Differential Transmit Data[8:0]. These signals are the positive signals of a differential pair used to transmit the high speed 8-bits of information to the CRUSH 11/12 (North Bridge).
LDT_TXD[8:0]#	DIFF OUT	LDT Link Negative Differential Transmit Data[8:0]. These signals are the negative signals of a differential pair used to transmit the high speed 8-bits of information to the CRUSH 11/12 (North Bridge).

5.2 PCI Bus Interface

Signal	I/O	Definition
PCI_AD[31:0]	I/O	PCI Address / Data Bus. A bus transaction consists of an address phase followed by one or more data phases. When PCI_FRAME# is asserted (first clock of a PCI transaction), the physical address (32-bits) is driven. During subsequent clocks, data is driven or received.
PCI_CBE[3:0]#	I/O	PCI Command / Byte Enables. During the address phase of a transaction, these signals define the PCI bus command. During the data phase, these signals are used as the byte enables corresponding to the supplied or requested data. The byte enables are valid for the entire data phase and determine which byte lanes contain valid data.
PCI_CLK[5:0]	O	PCI Clock Out[5:0]. These signals are the six in-phase 33MHz PCI bus clock outputs. They are intended for the five external PCI slots and one to loop back for the MCP-1. It provides the timing reference for all transactions on the PCI bus.
PCI_CLKFB	I	PCI Clock Feed Back. This signal is one of the 33MHz PCI_CLK[5:0] signal that is looped back into the MCP-1 to be used internally.
PCI_DEVSEL#	I/O	PCI Device Select. When acting as an output, it indicates that the MCP-1 has decoded the PCI address and is claiming the current access as the target. As an input, it indicates whether any other device on the bus has accepted the current transaction.
PCI_FRAME#	I/O	PCI Cycle Frame. This signal is driven by the current master to indicate the beginning and duration of an access. It is asserted to indicate that a bus transaction is beginning and that it is in the address phase. Data transfers can continue while it is asserted. When it is de-asserted, the transaction is in the final data phase.
PCI_GNT[4:0]#	O	PCI Slot Grant. This signal is asserted by the MCP-1 to grant the PCI bus to a requesting PCI bus Master device. GPIO1. When PCI_GNT[4] is not selected, it becomes GPIO1.
PCI_INT[E:A]#	I	PCI Slot Interrupt. This signal is generated by a PCI device on any of the 5 external PCI slots to indicate that it needs service. GPIO3. When PCI_INT[E] is not selected, it becomes GPIO3.
PCI_IRDY#	I/O	PCI Initiator Ready. This signal indicates the initiator's ability to complete the current data phase of the transaction. It is asserted from the first clock cycle after PCI_FRAME# is asserted to the last clock cycle of the PCI transaction. It is used in conjunction with PCI_TRDY#. Data is transferred on each PCI_CLK in which both PCI_IRDY# and PCI_TRDY# are sampled asserted. Wait states are inserted until both PCI_IRDY# and PCI_TRDY# are asserted together. During a write cycle, PCI_IRDY# indicates the MCP-1 has valid data on PCI_AD[31:0]. During a read cycle, it indicates the MCP-1 is ready to latch data.
PCI_PAR	I/O	PCI Parity. This signal is the even parity bit generated across PCI_AD[31:0] and PCI_CBE[3:0]#. It is stable and valid one clock after the address phase. It is stable and valid one clock after each write data phase. It is stable and valid one clock after each read phase is completed.
PCI_PERR#	I/O	PCI Parity Error. This signal is driven by an external PCI device when it receives data that has parity error. The MCP-1 drives this signal when it detects a parity

		error. GPIO2. When this function is not selected, it becomes GPIO2.
PCI_REQ[4:0]#	I	PCI Slot Interrupt Requests. This signal is generated by a PCI device on any of the 5 external PCI slots to request an Interrupt to the MCP-1. GPIO0. When PCI_REQ[4] is not selected, it becomes GPIO0.
PCI_RESET#	O	PCI Reset. This signal is asserted by the MCP-1 to reset devices that reside on the PCI bus. The MCP-1 asserts this signal during power up and when S/W initiates a hard reset sequence.
PCI_SERR#	I	PCI System Error. This signal can be asserted active for one clock cycle by any PCI device that detects a system error condition. A system error condition can be an address or data parity error on a special cycle command. It has no timing relationship to a PCI transaction. It is a synchronous signal.
PCI_STOP#	I/O	PCI Stop. This signal indicates that the current target is requesting the initiator to stop the current PCI transaction. It is an output when the MCP-1 is the target and an input when the MCP-1 is the initiator.
PCI_TRDY#	I/O	PCI Target Ready. This signal indicates the target's ability to complete the current data phase of the transaction. It is used in conjunction with PCI_IRDY#. A data phase is completed when both PCI_TRDY# and PCI_IRDY# are sampled asserted. Wait states are inserted until both PCI_IRDY# and PCI_TRDY# are asserted together. During a read cycle, it indicates that the target, has placed valid data on PCI_AD[31:0]. During a write cycle, it indicates the target has latched the data. PCI_TRDY# is an input to the MCP-1 when the MCP-1 is the initiator and an output from the MCP-1 when the MCP-1 is the target.

5.3 Primary IDE Interface

Signal	**I/O**	**Definition**
IDE_ADDR_P[2:0]	O	Primary IDE Address. This signal is the IDE controller's primary port address. It indicates which byte in either the ATA command or control register block is being addressed.
IDE_CS1_P#	O	Primary Port Chip Select 1xx. This signal is the primary port chip select for 1F7h – 1F0h range. It is used for the AT command register block.
IDE_CS3_P#	O	Primary Port Chip Select 3xx. This signal is the primary port chip select for 3F7h – 3F4h range. It is used for the AT control register block.
IDE_DACK_P#	O	Primary DMA Acknowledge. This signal is the DMA acknowledge of the primary IDE channel. The MCP-1 responds to the IDE_DRQ_P signal from a primary IDE device either to acknowledge that the DMA data has been accepted or to inform that DMA data is available.
IDE_DATA_P[15:0]	I/O	Primary Data Bus. These signals are the bi-directional data bus used to transfer data to or from the primary IDE device. When the MCP-1 is writing to a primary IDE device, they are driven valid before the negation of the IDE_IOW_P# signal. When the MCP-1 is reading from a primary IDE device, they are sampled at the rising edge of IDE_IOR_P# signal. They are tri-stated when no read or write is in process.

IDE_DRQ_P	I	Primary DMA Request. This signal is the DMA request signal from the primary IDE channel. When ready to read or write DMA data, the primary IDE device asserts this signal.
IDE_INTR_P	I	Primary Interrupt. This signal is the Interrupt signal from the primary IDE device to request service.
IDE_IOR_P#	O	Primary I/O Read. This signal is the primary IDE channel read strobe for PIO and DMA modes. The falling edge of this signal enables the transfer of data from a register or data port of the device onto IDE_DAT_P[15:0]. Primary Ultra DMA Host Ready. This signal is the primary channel flow control for Ultra DMA input data bursts. When ready to receive DMA data, a primary IDE host asserts this signal. The primary IDE host may stop toggling this signal to pause an Ultra DMA input data transfer. Primary Ultra DMA Host Strobe. This signal is the primary channel strobe signal from the host for an Ultra DMA output data transfer. Both edges of this signal latch data from IDE_DAT_P[15:0] into the device. The host may stop toggling this signal to pause an Ultra DMA output data transfer.
IDE_IOW_P#	O	Primary I/O Write. This signal is the primary IDE channel write strobe for PIO and DMA modes. The rising edge of this signal latches IDE_DAT_P[15:0] into either a register or data port of the device. Primary Stop. This signal is the primary IDE channel stop for Ultra DMA modes. It halts the data transfer of the primary IDE channel.
IDE_RDY_P	I	Primary Device Ready. This signal is the primary channel IDE device ready indicator for PIO modes. If a device is not ready to respond to a data transfer request, the device negates this signal to extend the read or write cycle. When negated, this signal is in a high impedance state. Primary Ultra DMA Device Ready. This signal is the primary channel flow control signal for Ultra DMA output data bursts. When ready to receive DMA data, a primary IDE device asserts this signal. The primary IDE device negates this signal to pause an Ultra DMA output data transfer. Primary Ultra DMA Device Strobe. This signal is the primary channel input data strobe signal from the primary IDE device for an Ultra DMA input data transfer. Both edges of this signal latch data from IDE_DAT_P[15:0] into the host. The primary IDE device may stop toggling this signal to pause an Ultra DMA data in transfer.

5.4 Secondary IDE Interface

Signal	**I/O**	**Definition**
IDE_ADDR_S[2:0]	O	Secondary IDE Address. This signal is the IDE controller's secondary port address. It indicates which byte in either the ATA command or control register block is being addressed.
IDE_CS1_S#	O	Secondary Port Chip Select 1xx. This signal is the secondary port chip select for 1F7h – 1F0h range. It is used for the AT command register block.
IDE_CS3_S#	O	Secondary Port Chip Select 3xx. This signal is the secondary port chip select for 3F7h – 3F4h range. It is used for the AT control register block.
IDE_DACK_S#	O	Secondary DMA Acknowledge. This signal is the DMA acknowledge of the secondary IDE channel. The MCP-1 responds to the IDE_DRQ_S signal from a secondary IDE device either to acknowledge that the DMA data has been accepted or to inform that DMA data is available.

IDE_DATA_S[15:0]	I/O	Secondary Data Bus. These signals are the bi-directional data bus used to transfer data to or from the secondary IDE device. When the MCP-1 is writing to a secondary IDE device, they are driven valid before the negation of the IDE_IOW_S# signal. When the MCP-1 is reading from a secondary IDE device, they are sampled at the rising edge of IDE_IOR_S# signal. They are tri-stated when no read or write is in process.
IDE_DRQ_S	I	Secondary DMA Request. This signal is the DMA request signal from the secondary IDE channel. When ready to read or write DMA data, the secondary IDE device asserts this signal.
IDE_INTR_S	I	Secondary Interrupt. This signal is the Interrupt signal from the secondary IDE device to request service.
IDE_IOR_S#	O	Secondary I/O Read. This signal is the secondary IDE channel read strobe for PIO and DMA modes. The falling edge of this signal enables the transfer of data from a register or data port of the device onto IDE_DAT_S[15:0]. Secondary Ultra DMA Host Ready. This signal is the secondary channel flow control for Ultra DMA input data bursts. When ready to receive DMA data, a secondary IDE host asserts this signal. The secondary IDE host may stop toggling this signal to pause an Ultra DMA input data transfer. Secondary Ultra DMA Host Strobe. This signal is the secondary channel strobe signal from the host for an Ultra DMA output data transfer. Both edges of this signal latch data from IDE_DAT_S[15:0] into the device. The host may stop toggling this signal to pause an Ultra DMA output data transfer.
IDE_IOW_S#	O	Secondary I/O Write. This signal is the secondary IDE channel write strobe for PIO and DMA modes. The rising edge of this signal latches IDE_DAT_S[15:0] into either a register or data port of the device. Secondary Stop. This signal is the secondary IDE channel stop for Ultra DMA modes. It halts the data transfer of the secondary IDE channel.
IDE_RDY_S	I	Secondary Device Ready. This signal is the secondary channel IDE device ready indicator for PIO modes. If a device is not ready to respond to a data transfer request, the device negates this signal to extend the read or write cycle. When negated, this signal is in a high impedance state. Secondary Ultra DMA Device Ready. This signal is the secondary channel flow control signal for Ultra DMA output data bursts. When ready to receive DMA data, a secondary IDE device asserts this signal. The secondary IDE device negates this signal to pause an Ultra DMA output data transfer. Secondary Ultra DMA Device Strobe. This signal is the secondary channel input data strobe signal from the secondary IDE device for an Ultra DMA input data transfer. Both edges of this signal latch data from IDE_DAT_S[15:0] into the host. The secondary IDE device may stop toggling this signal to pause an Ultra DMA data in transfer.

5.5 IEEE 802.3 MAC Interface (MII)

Signal	I/O	Definition
MII_COL	I	MII_Collision. This signal is asserted by the PHY upon detection of a collision condition on the medium. It remains asserted while the collision condition persists. It is asserted by a PHY that is operating at 10Mb/s in response to a *signal_quality_error*. It is not required to transition synchronously with respect to either the MII_TXCLK or the MII_RXCLK. HPNA 1.0/2.0: This signal is not used in HPNA 1.0/2.0.
MII_CRS	I	MII_Carrier Sense. This signal is asserted by the PHY when either the transmit or receive medium is non-idle. It is de-asserted by the PHY when both the transmit and receive media are idle. It remains asserted throughout the duration of a collision condition. It is not required to transition synchronously with respect to either the MII_TXCLK or the MII_RXCLK. HPNA 1.0/2.0: On transmit; the PHY asserts this signal some time after MII_TXEN is asserted. It is de-asserted after MII_TXEN is de-asserted AND when the PHY is ready to receive another packet. When this signal is de-asserted, the MAC times out an IFG (0.96usec) and may asserted MII_TXEN again if there is another packer to send. On receive, the PHY asserts this signal to seize the half-duplex MII channel, waits a short time (an IFG), then may wait for MII_TXEN (which may just have been asserted) to de-assert plus an IFG, and then raises MII_RXDV to transfer the packet. At the end of the transfer, it de-asserts this signal unless the transmit buffer is full or there is another receive packet ready to transfer.
MII_MDC	O	MII_Management Data Clock. This signal is used as the timing reference for transfer of information on the MII_MDIO signal. This signal is an a-periodic signal that has no maximum high or low times. The minimum high and low time is 160nsec each, and the minimum period for it is 400nsec, regardless of the nominal period of MII_TXCLK and MII_RXCLK.
MII_MDIO	I/O	MII_Management Data I/O. This signal is a bi-directional signal between the PHY and the STA. It is used to transfer control information and status between. Control information is driven by the STA synchronously with respect to MII_MDC and is sampled by the PHY. Status information is driven by the PHY synchronously with respect to MII_MDC and is sampled by the STA.
MII_RXCLK	I	MII_Received Clock. This signal is a continuous clock that provides the timing reference for the transfer of the MII_RXDV, MII_RXD[3:0], and MII_RXER signals.
MII_RXD[3:0]	I	MII_Received Data [3:0]. These signals transfer four bits of recovered data for each M_RXCLK period when M_RXDV is asserted. M_RXD[0] is the least significant bit. While M_RXDV is de-asserted, these signals shall have no effect on the MAC. It transitions synchronously with respect to M_RXCLK.
MII_RXDV	I	MII_Received Data Valid. This signal is driven by the PHY to indicate that it is presenting recovered and decoded data on the MII_RXD[3:0] lines and that the data is synchronous to MII_RXCLK. This signal transitions synchronously with respect to MII_RXCLK. This signal remains asserted continuously from the first recovered MII_RX[3:0] of the frame through the final recovered MII_RX[3:0] and it is negated prior to the first MII_RXCLK that follows the final MII_RX[3:0]. In order for a received frame to be correctly interpreted by the

		MAC, MII_RXDV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding and End-of-Frame Delimiter.
MII_RXER	I	MII_Receive Error. This signal is asserted for one or more MII_RXCLK periods to indicate to the MAC that an error was detected somewhere in the frame presently being transferred from the PHY. This signal transitions synchronously with respect to MII_RXCLK. While MII_RXDV is de-asserted, the PHY may provide a False Carrier indication by asserting this signal for at least one cycle of MII_RXCLK while driving the appropriate value onto MII_RXD[3:0]. GPIO4. When MII_RXER function is not selected, it becomes GPIO4.
MII_TXCLK	I	MII_Transmit Clock. This signal is a continuous clock that provides the timing reference for the transfer of the MII_TX_EN and MII_TXD[3:0] signals.
MII_TXD[3:0]	O	MII_Transmit Data [3:0]. These signals transfer four bits of data to the PHY for each MII_TXCLK period when MII_TXEN is asserted. MII_TXD[0] is the least significant bit. While MII_TXEN is de-asserted, these signals will have no effect upon the PHY. These signals transition synchronously with respect to MII_TXCLK.
MII_TXEN	O	MII_Transmit Data Enable. This signal indicates that the MAC is presenting valid data on MII_TXD[3:0] on the MII channel for transmission. This signal is asserted by the MAC synchronously with the first MII_TXD[3:0] for the preamble and shall remain asserted while all MII_TXD[3:0] to be transmitted are presented on the MII channel. This signal is negated prior to the first MII_TXCLK following the final MII_TXD[3:0] of a frame.

5.6 CPU Interface

Signal	I/O	Definition
A20GATE	I	A20 Gate. This signal is the sum of the keyboard controller A20GATE signal and port 92h register. This signal is connected directly to the A20M# pin on the processor. GPIO12. When this function is not selected, it becomes GPIO12.
A20M#	OD	Mask A20. This signal is the mask of processor address bit [20] to the processor. It is used for Frequency Strapping. It is an Open-Drain signal and only actively driven low.
APIC_CLK	I	APIC Clock. This signal is the I/O APIC interface clock used to transmit data to and from the CPU's Local APIC controller.
APIC_DATA[1:0]#	I/O	APIC Data. These bi-directional signals are used to send and received data over the APIC bus. As inputs, the data is valid on the rising edge of APIC_CLK. As outputs, new data is driven from the rising edge of APIC_CLK.
CPU_RST#	I	CPU Reset. This signal is sampled to determine when to release the Frequency Strapping settings to the processor.
CPU_VREF	A	CPU Reset Voltage Reference. This signal is used to set the threshold level for the CPU_RST# signal.
FERR#	I	Floating Point Error. This signal is generated by the processor to indicate that the execution of a floating-point instruction caused an unmasked floating-point exception. This signal is tied to the FERR# signal on the processor. If this signal is asserted, the MCP-1 generates an internal IRQ13 to its interrupt controller unit and asserts INTR. It is also used to gate the IGNNE# signals to ensure that IGNNE# is not asserted to the processor unless FERR# is active.
IGNNE#	OD	Ignore Numeric Error. This signal is asserted on a write to port F0h (Coprocessor Error Register) ONLY when FERR# is asserted. This signal remains asserted until FERR# is de-asserted. This signal is connected to the ignore numeric exception pin on the processor. It is used for Frequency Strapping. This is an Open-Drain signal and only actively driven low.
INIT#	OD	CPU Initialization. This signal is asserted by the MCP-1 for to initialize the processor. It is an Open-Drain signal and only actively driven low.
INTR	OD	CPU Interrupt. This signal is asserted by the MCP-1 to signal the processor that an interrupt request is pending and needs to be serviced. It is used for Frequency Strapping. This is an Open-Drain signal and is only actively driven low.
NMI	OD	Non-Maskable Interrupt. This signal is used to force a non-maskable interrupt to the processor. An error on the NSL may be programmed to cause this to occur. It is used for Frequency Strapping. It is an Open-Drain signal and only actively driven low.
SMI#	OD	System Management Interrupt. This signal is asserted by the MCP-1 in response to one of many enabled events. It is an Open-Drain signal and only actively driven low.
STPCLK#	OD	Stop Clock. This signal is asserted by the MCP-1 in response to one of many hardware or software power management events to place the processor in a Stop Grant state. It is an Open-Drain signal and only actively driven low.

5.7 LPC Interface

Signal	I/O	Definition
LPC_AD[3:0]	I/O	LPC Multiplexed Command, Address, Data. These signals are used to communicate information such as; start, stop (abort a cycle), transfer type (memory, I/O, DMA), transfer direction (read/write), address, data, wait states, DMA channel, and bus master grant.
LPC_CLK	O	LPC Clock. This signal is the in-phase 33MHz PCI bus clock. It provides the timing reference for all transactions on the LPC bus.
LPC_DRQ[1:0]#	I	LPC Serial DMA/Master Requests. These signals are used by and external device to request DMA or bus master accesses when this function is selected. They are typically connected to an external Super I/O device. GPIO5. When LPC_DRQ1# function is not selected, it becomes GPIO5.
LPC_FRAME#	O	LPC Frame. This signal indicates the start of an LPC cycle or termination of a LPC cycle due to an abort or timeout.
SERIRQ#	I	LPC Serial Interrupt. This signal is the serial interrupt signal from the external LPC bus. It is used to transmit interrupt information to the internal interrupt controller.

5.8 USB Interface

Signal	I/O	Definition
USB_N[5:0]	DIFF I/O	USB Port[5:0] Negative Differential Signals. These signals are the negative differential output drivers that drive the USB port [5:0] data signals onto the USB cable. They support both the full speed (12Mbps) and low speed (1.5Mbps) data rates.
USB_P[5:0]	DIFF I/O	USB Port[5:0] Positive Differential Signals. These signal are the positive differential output drivers that drive the USB port [5:0] data signals onto the USB cable. They support both the full speed (12Mbps) and low speed (1.5Mbps) data rates.
USB_OC[5:0]#	I	USB Over-current Indicators. These signals set corresponding bits in the USB controller to indicate that an over-current condition has occurred per channel when this function is selected. GPIO[10:6]. When USB_OC[5:1]# function is not selected, it becomes GPIO[10:6].
USB_VREF	A	USB Voltage Reference. This signal is the voltage reference for the integrated USB differential drivers and receivers.

5.9 System and Power Management Interface

Signal	I/O	Definition
CPUSLP#	I/O	CPU Sleep. When this signal is connected to the processor's sleep pin, asserting it places the processor into a non-snoop-capable low power state. GPIO18. When this function is not selected, it becomes GPIO18.
EXTSMI#	I/O	External SMI. This signal can be used to generate SMI or SCI interrupts and resume events. This signal can be wired-OR. GPIO21. When this function is not selected, it becomes GPIO21.
FANCTL[1:0]	I/O	Fan Control. This signal is used to control the rate of system fans. GPIO[16:15]. When this function is not selected, it becomes GPIO[16:15].
FANRPM	I/O	Fan RPM. This signal can be used to track the RPM of the fan. GPIO14. When this function is not selected, it becomes GPIO14.
INTRUDER#	I/O	Intruder. This signal is an input that can be connected to a switch that is activated by opening the system chassis. When this input is asserted for more than 60usec, it can be enabled to cause an SCI or SMI interrupt. GPIO23. When this function is not selected, it becomes GPIO23.
KBRDRSTIN#	I/O	Keyboard Reset In. This signal functions as a reset input from the external keyboard controller that is used to generate a pulse on CPU_RST# or INIT#. GPIO25. When this function is not selected, it becomes GPIO25.
PME#	I/O	Power Management Event. This signal is used to generate SMI or SCI interrupt and resume events. This signal can be wired-OR.
PRDY#	I/O	Processor Ready. This signal is used to control the internal counters. GPIO17. When this function is not selected, it becomes GPIO17.
PWRBTN#	I/O	Power Button. When the system is in the Soft Off (G2) state, this signal controls the automatic transition to Full On (G0). It can be programmed to generate SCI or SMI interrupts from any state other than Soft Off (G2). If asserted for four seconds from any state other than Soft Off (G2), a power button override event is generated.
PWRGD	I	Power Good. When this signal is asserted, it is an indication to the MCP-1 that core power and PCI_CLK[5:0] have been stable for at least 1msec. This signal can be driven asynchronously. When this signal is negated, the MCP-1 asserts PCI_RESET#.
PWRGD_SB	I	Power Good Standby. This signal is connected to a signal that goes active when the standby power supply is stable. It is used to reset the logic on this power plane.
RI#	I/O	Ring Indicator. This signal can be connected to an external modem circuitry to allow the system to be re-activated by a phone call. It causes the system to resume

		to the Full On (G0) state and generates SCI or SMI interrupts. GPIO24. When this function is not selected, it becomes GPIO24.
SLP_S1#	I/O	Sleep State S1. This signal is asserted when the power state machine is in the S1 state or lower. This can be used to control power planes. GPIO20. When this function is not selected, it becomes GPIO20.
SLP_S3#	I/O	Sleep State S3. This signal is asserted when the power state machine is in the S3 state or lower. This can be used to control power planes.
SLP_S5#	I/O	Sleep State S5. This signal is asserted when the power state machine is in the S5 state. This can be used to control power planes.
SLPBTN#	I/O	Sleep Button. This signal causes the system to transition between Sleep (G1/G2) and Full On (G0) states. GPIO19. When this function is not selected, it becomes GPIO19.
THERM#	I/O	Thermal. This signal can be enabled to automatically result in CPU throttling when an even has occurred. GPIO22. When this function is not selected, it becomes GPIO22.

5.10 Audio/Modem Interface (AC ’97 AC-Link)

Signal	**I/O**	**Definition**
AC_BITCLK	I	AC-Link Clock. This signal is the AC ‘97 12.288MHz clock used for serial data transfer between the CODEC and MCP-1. This clock is also used for S/PDIF_OUT.
AC_RESET#	O	AC-Link Reset. This signal is the active low AC ’97 reset signal.
AC_SDATA_OUT	O	AC-Link Serial Data Out. This signal is the serial, time division multiplexed, AC ’97 output data stream to the CODEC.
AC_SDATA_IN0	I	AC-Link Serial Primary Data In. This signal is the serial, time division multiplexed, AC ’97 input data stream from the primary CODEC.
AC_SDATA_IN1	I	AC-Link Serial Secondary Data In. This signal is the serial, time division multiplexed, AC ’97 input data stream from the secondary CODEC when AC-Link is selected. GPIO11. When this function is not selected, it becomes GPIO11.
AC_SYNC	O	AC-Link Synchronization. This signal is the fixed AC ’97 48KHz synchronization signal between the MCP-1 and CODEC.

5.11 Dual SMBus and DDC Interface

Signal	I/O	Definition
DDC_CLK	I/O	DDC Clock. This signal is the DDC Clock when DDC bus is selected. SPIO4. When DDC bus is not selected, then it becomes SPIO4.
DDC_DATA	I/O	DDC Data. This signal is the DDC Data when DDC bus is selected. SPIO5. When DDC bus is not selected, then it becomes SPIO5.
SMB_DATA[1:0]	I/O	SMBus Data[1:0]. These signals are the two System Management Bus Data when SMBus is selected. SPIO[3,1]. When SMBus is not selected, then it becomes SPIO[3,1].
SMB_CLK[1:0]	I/O	SMBus Clock[1:0]. These signals are the two System Management Bus Clock when SMBus is selected. SPIO[2,0]. When SMBus is not selected, then it becomes SPIO[2,0].
SMB_ALERT#	I	SMBus Alert. This signal is used generate an SMI# or interrupt associated with the SMBus logic when SMBus is selected. SPIO6. When SMBus is not selected, then it becomes SPIO6.

5.12 Clocks

Signal	I/O	Definition
BUF_14M	O	Buffered 14.31818MHz. This signal is a buffered version of the 14.31818MHz crystal that is used internally by the MCP-1 and sent to the CRUSH 11/12.
BUF_24M	O	Buffered 24MHz. This signal is used as the FDC clock for the Super IO.
RTC_XI	A	Crystal Input 0. This signal can be connected to the 32.768KHz crystal. It can also be driven by a CMOS clock driver with a 32.768KHz frequency.
RTC_XO	A	Crystal Input 1. This signal is connected to the 32.768KHz crystal. This pin is a no connect when RTCXI is driven by a CMOS clock driver.
XTAL_14M_IN	A	14.31818MHz Crystal Input. This signal is used by the internal clock synthesizer to generate all internal clocks. It is connected to the 14.31818MHz crystal. It can also be driven by a CMOS clock driver with a 14.31818MHz frequency.
XTAL_14M_OUT	A	14.31818MHz Crystal Output. This signal is connected to the 14.31818MHz crystal. This pin is a no connect when XTAL_14M_IN is driven by a CMOS clock driver.

5.13 Miscellaneous Interface

Signal	I/O	Definition
SPDIF	O	S/PDIF Output. This signal is used to transmit 48KHz stereo or AC-3 data to an external S/PDIC receiver when this function is selected. GPIO13. When S/PDIF function is not selected, it becomes GPIO13.
SPKR	O	Speaker. This signal is the output of counter 2. This signal drives an external speaker driver, which in turn drives the system speaker.
TEST	I	Test. This signal is sampled on the rising edge of PWRGD_SB and is used to place the device into a test mode. It should be connected to GND through a 1KΩ resistor for normal operation.

5.14 Power Interface

Signal	Power	I/O	Definition
VDD_PLL	3.3V	P	Filter PLL Power. This voltage is the filter supply connected to the internal PLL used to generate the various clocks.
VDD_AUXC	1.2V	P	Sleep Mode 1.2V Core Power. This voltage is used to power the internal power management circuitry.
VBATT	1.2V	P	1.2V Battery Voltage. This voltage is connected to the RTC.
VDD	1.2V	P	1.2V Core Power. This voltage powers the MCP-1 core.
VDD_3P3	3.3V	P	3.3V Power. This voltage is used to power the 3.3V interface to 3.3V peripherals.
VDD_5	5V	P	5V Power. This voltage is used as the reference voltage for the 5V tolerant I/O.
VDD_AUX3	3.3V	P	Sleep Mode 3.3V. This voltage is used to power the power management interface to 3.3V peripherals.
VDD_AUX5	5V	P	Sleep Mode 5V. This voltage is used to power the power management interface to 5V peripherals.
VDD_LDT	1.2V	P	1.2V LDT Power. This voltage powers the LDT interface.
VDD_USB	3.3V	P	3.3V USB Power. This voltage powers the internal dual USB controllers.
CPU_VTT	1.5-1.7V	P	CPU Interface Power. This power plane is used for the CPU interface signals.
GND		P	Ground.

5.15 Multiplexed Pins

Multiplexed GPIO/SPIO Pins:

The MCP-1 has 33 multiplexed signal and GPIO/SPIO pins. Table 1 below lists signal pins and their corresponding GPIO/SPIO pins. There are 26 GPIO pins and 7 SPIO pins. GPIO and SPIO are the same function, but have different control mechanisms. The GPIO[25:0] (PMD9:PMC0) and SPIO[6:0] (GPC6:GPC0) registers control whether the pins are the default signal functions or are GPIO/SPIO functions. When selected for GPIO/SPIO functions, the registers also select whether the pins are inputs, outputs, interrupt generators, or bus controls. There is one register for each pin that controls the state of each pin.

Table 1. GPIO/SPIO Pins

GPIO/SPIO	Control Register	Signal Name
GPIO0	PMC0	PCI_REQ4#
GPIO1	PMC1	PCI_GNT4#
GPIO2	PMC2	PCI_PERR#
GPIO3	PMC3	PCI_INTRE
GPIO4	PMC4	MII_RXER_P
GPIO5	PMC5	LPC_DRQ1
GPIO6	PMC6	USB_OC1
GPIO7	PMC7	USB_OC2
GPIO8	PMC8	USB_OC3
GPIO9	PMC9	USB_OC4
GPIO10	PMCA	USB_OC5
GPIO11	PMCB	AC_SDATA_IN1
GPIO12	PMCC	A20GATE
GPIO13	PMCD	SPDIF_OUT
GPIO14	PMCE	FANRPM
GPIO15	PMCF	FANCON0
GPIO16	PMD0	FANCON1
GPIO17	PMD1	PRDY#
GPIO18	PMD2	CPUSLP#
GPIO19	PMD3	SLPBTN#
GPIO20	PMD4	SLP_S1#
GPIO21	PMD5	EXTSMI#
GPIO22	PMD6	THERM#
GPIO23	PMD7	INTRUDER#
GPIO24	PMD8	RI#
GPIO25	PMD9	KBRDRSTIN#
SPIO0	GPC0	SMB_CLK0
SPIO1	GPC1	SMB_DAT0
SPIO2	GPC2	SMB_CLK1
SPIO3	GPC3	SMB_DATA1
SPIO4	GPC4	DDC_CLK
SPIO5	GPC5	DDC_DATA
SPIO6	GPC6	SMB_ALERT#

As a GPIO pin, these pins have the following options:

Outputs – Can be set HIGH or LOW.
Can be controlled by GPIO output clocks 0 or 1.

Inputs – Active HIGH or LOW programmable.
SCI or SMI IRQ capable
Can be latched or not latched
Can be de-bounce protected

There are two GPIO output clocks (numbered 0 and 1). They are specified by PMBC. Each output clock includes a 7-bit programmable high time, a 7-bit programmable low time, and the counter can be clocked by one of four frequencies.

PMBC[CLK[1,0]BASE]	Base Clock Period	Output High Time	Output Low Time
‘b00	250usec	250usec-to-32msec	250usec-to-32msec
‘b01	2msec	2msec-to-256msec	2msec-to-256msec
‘b10	16msec	16msec-to-2sec	16msec-to-2sec
‘b11	128msec	128msec-to-16.4sec	128msec-to-16.4sec

The output of the two GPIO output clocks can be selected to drive the output of any of the GPIO pins.

5.16 Strapping Pins

The MCP uses the following pins for Strapping Options:

Pin Strap	Function	Strapped Value
SPKR	Reserved	Must be pulled-up HIGH through a resistor.
SPDIF	Reserved	Must be pulled-up HIGH through a resistor.
AC_SDATA_OUT	Reserved	Must be pulled-down LOW through a resistor.
MII_MDC	Reserved	Must be pulled-down LOW through a resistor.

While PWRGD is asserted low, these outputs will become inputs. When PWRGD goes high, their value is latched internally and used to configure the device.

5.17 Power Planes

The MCP-1 uses 12 different power planes as described in the Table below. They are connected to the various power supply pins described in the Power Interface Pin Description section. The 12 different power planes are used for the various functions of the MCP-1 as described in the Power Plane Connections tables below.

Signal	Power	Definition
CPU_VTT	1.5-1.7V	CPU Interface Power. This power plane is used for the CPU interface signals.
VDD_PLL	3.3V	Auxiliary 3.3V PLL Power. This power plane is the filter version of the VDD_3P3 supply connected to the internal PLL.
VDD_AUXC	1.2V	Auxiliary 1.2V Core Power. This power plane is for the MCP-1 core power management circuitry.
VBATT	1.2V	1.2V RTC Battery Back-up Power. This power plane is for the battery backed-up Real Time Clock.
VDD	1.2V	1.2V Core Power. This power plane is for the MCP-1 core.
VDD_3P3	3.3V	3.3V Power. This power plane provides I/O power for interfaces to 3.3V peripherals.
VDD_2P5	2.5V	2.5V Power. This power plane is for the CPU and CRUSH 11/12 (North Bridge).
VDD_5	5V	5V Power. This power plane protects the MCP-1 I/O pads from 5V peripherals.
VDD_AUX3	3.3V	Auxiliary 3.3V. This power plane is for the power management circuitry interfacing to 3.3V peripherals.
VDD_AUX5	5V	Auxiliary 5V. This power plane is for the power management circuitry interfacing to 5V peripherals.
VDD_LDT	1.2V	1.2V LDT Power. This power plane is for the LDT Interface.
VDD_USB	3.3V	3.3V USB Power. This power plane is for the two integrated USB controllers.

5.18 Power Plane Connections

LDT Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
LDT_RSET	VDD_LDT	VDD_LDT	1.2	1.2
LDT_RST#	VDD_LDT	VDD_LDT	2.5	2.5
LDT_RXD[8:0]	VDD_LDT	VDD_LDT	1.2	1.2
LDT_RXD[8:0]#	VDD_LDT	VDD_LDT	1.2	1.2
LDT_RXCLK	VDD_LDT	VDD_LDT	1.2	1.2
LDT_RXCLK#	VDD_LDT	VDD_LDT	1.2	1.2
LDT_TXD[8:0]	VDD_LDT	VDD_LDT	1.2	1.2
LDT_TXD[8:0]#	VDD_LDT	VDD_LDT	1.2	1.2
LDT_TXCLK	VDD_LDT	VDD_LDT	1.2	1.2
LDT_TXCLK#	VDD_LDT	VDD_LDT	1.2	1.2

PCI Bus Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
PCI_AD[31:0]	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_C/BE[3:0]#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_DEVSEL#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_FRAME#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_INT[E:A]#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_IRDY#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_PAR	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_CLK[5:0]	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
PCI_CLK_IN	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
PCI_GNT[4:0]#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_PERR#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_REQ[4:0]#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_RESET#	VDD_AUX3	VDD_5 or VDD_3P3	3.3	3.3
PCI_SERR#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_STOP#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
PCI_TRDY#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3

Primary IDE Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
IDE_ADDR_P[2:0]	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_CS1_P#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_CS3_P#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_DACK_P#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_DATA_P[15:0]	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
IDE_DRQ_P#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
IDE_INTR_P	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
IDE_IOR_P#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_IOW_P#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_RDY_P#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3

Secondary IDE Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
IDE_ADDR_S[2:0]	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_CS1_S#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_CS3_S#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_DACK_S#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_DATA_S[15:0]	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
IDE_DRQ_S#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
IDE_INTR_S	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
IDE_IOR_S#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_IOW_S#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
IDE_RDY_S#	VDD_3P3	VDD_5 or VDD_3P3	5	3.3

Dual SMBus and Dual DDC Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
SMB_DATA[1:0]	VDD_AUX3	VDD_3P3	5	3.3
SMB_CLK[1:0]	VDD_AUX3	VDD_3P3	5	3.3
SMB_ALERT#	VDD_AUX3	VDD_3P3	5	3.3
DDC_CLK	VDD_3P3	VDD_3P3	5	3.3
DDC_DATA	VDD_3P3	VDD_3P3	5	3.3

IEEE 802.3 MAC Interface (MII)				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
MII_COL	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_CRS	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_MDIO	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_MDC	VDD_AUX3	VDD_5 or VDD_3P3	3.3	3.3
MII_RXCLK	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_RXD[3:0]	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_RXDV	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_RXER	VDD_AUX3	VDD_5 or VDD_3P3	5	3.3
MII_TXCLK	VDD_3P3	VDD_5 or VDD_3P3	5	3.3
MII_TXD[3:0]	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
MII_TXEN	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3

LPC Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
LPC_AD[3:0]	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
LPC_CLK	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
LPC_DRQ[1:0]#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
LPC_FRAME#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
SERIRQ#	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3

USB Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
USB_P[5:0]	VDD_USB	VDD_5	3.3	3.3
USB_N[5:0]	VDD_USB	VDD_5	3.3	3.3
USB_OC[5:0]#	VDD_AUX3	VDD_5 or VDD_3P3	3.3	3.3
USB_VREF			3.3	3.3

Audio/Modem Interface (AC ’97 AC-Link)				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
AC_SYNC	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
AC_BITCLK	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
AC_SDATA_OUT	VDD_3P3	VDD_5 or VDD_3P3	3.3	3.3
AC_SDATA_IN0	VDD_AUX3	VDD_5 or VDD_3P3	3.3	3.3
AC_SDATA_IN1	VDD_AUX3	VDD_5 or VDD_3P3	3.3	3.3
AC_RESET#	VDD_AUX3	VDD_5 or VDD_3P3	3.3	3.3

Clocks				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
BUF_14.318	VDD_AUX3		3.3	3.3
BUF_24M	VDD_3P3		3.3	3.3
RTC_XI	VBATT			
RTC_XO	VBATT			
VDD_PLL	VDD_AUX3		3.3	3.3
VBATT	VBATT			
XTAL_14M_IN	VDD_AUX3		3.3	3.3
XTAL_14M_OUT	VDD_AUX3		3.3	3.3

CPU Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
A20GATE	VDD_3	VDD_3	3.3	3.3
A20M#	VTT_VREF	VTT_VREF		
APIC_CLK	VDD_2P5	VDD_2P5		
APIC_DATA[1:0]#	VTT_VREF	VTT_VREF		
CPU_RST#	VTT_VREF	VTT_VREF		
FERR#	VTT_VREF	VTT_VREF		
IGNNE#	VTT_VREF	VTT_VREF		
INIT#	VTT_VREF	VTT_VREF		
INTR	VTT_VREF	VTT_VREF		
NMI	VTT_VREF	VTT_VREF		
SMI#	VTT_VREF	VTT_VREF		
STPCLK#	VTT_VREF	VTT_VREF		

System and Power Management Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
CPUSLP#	VTT_VREF	VTT_VREF		
EXTSMI#	VDD_AUX3	VDD_AUX3	3.3	3.3
FANRPM	VDD_3P3	VDD_3P3	3.3	3.3
FANCTL[1:0]	VDD_3P3	VDD_3P3	3.3	3.3
INTRUDER#	VDD_AUX3	VDD_AUX3	3.3	3.3
KBRDRSTIN#	VDD_3P3	VDD_3P3	3.3	3.3
PME#	VDD_AUX3	VDD_AUX3	3.3	3.3
PRDY#	VTT_VREF	VTT_VREF		
PWRBTN#	VDD_AUX3	VDD_AUX3	3.3	3.3
PWRGD	VDD_AUX3	VDD_AUX3	3.3	3.3
PWRGD_SB	VDD_AUX3	VDD_AUX3	3.3	3.3
RI#	VDD_AUX3	VDD_AUX3	3.3	3.3
SLP_S1#	VDD_3P3	VDD_3P3	3.3	3.3
SLP_S3#	VDD_AUX3	VDD_AUX3	3.3	3.3
SLP_S5#	VDD_AUX3	VDD_AUX3	3.3	3.3
SLPBTN#	VDD_AUX3	VDD_AUX3	3.3	3.3
THERM#	VDD_3P3	VDD_3P3	3.3	3.3

Miscellaneous Interface				
Signal	**Source Power Plane**	**Destination Power Plane**	**Voltage Tolerance (V)**	**Voltage Drive (V)**
SPDIF	VDD_3P3	VDD_3P3	3.3	3.3
SPKR	VDD_3P3	VDD_3P3	3.3	3.3
TEST	VDD_3P3	VDD_3P3	3.3	3.3

6.0 MCP Ball Out

6.1 MCP-1 Ball Diagram

	1	2	3	4	5	6	7	8	9	10	11
A	SMB_CLK0	SMB_DATA0	SMB_CLK1	VDD_5	IDE_ADDR_S0	IDE_DACK_S#	GND	IDE_DATA_S15	IDE_DATA_S12	VDD_3P3	IDE_DATA_S8
B	RTC_XO	GND	SMB_DATA1	IDE_CS3_S#	IDE_ADDR_S2	IDE_INTR_S	IDE_IOR_S#	IDE_DATA_S0	IDE_DATA_S3	IDE_DATA_S5	IDE_DATA_S7
C	RTC_XI	VBATT	SMB_ALERT#	VDD_AUX5	IDE_CS1_S#	IDE_RDY_S#	IDE_IOW_S#	IDE_DATA_S1	IDE_DATA_S13	IDE_DATA_S10	IDE_CS1_P#
D	GND	INTRUDER	VDD_AUX3	GND	GND	VDD_3P3	VDD_3P3	IDE_DATA_S2	IDE_DATA_S4	GND	IDE_CS3_P#
E	XTAL_14M_OUT	VDD_PLL	NMI	GND	GND	IDE_ADDR_S1	IDE_DRQ_S	IDE_DATA_S14	IDE_DATA_S11	IDE_DATA_S6	IDE_DATA_S9
F	XTAL_14M_IN	INTR	SMI#	CPU_VTT	CPUSLP#						
G	APIC_DATA1	APIC_DATA0	INIT#	CPU_VTT	FERR#						
H	GND	LDT_RSET	STPCLK#	A20M#	IGNNE#						
J	LDT_RXD0#	LDT_RXD0	LDT_RXD4	LDT_RXD1	LDT_RXD1#				VDD	VDD	GND
K	LDT_RXCK#	LDT_RXCK	LDT_RXD4#	GND	LDT_RXD5				VDD	GND	GND
L	VDD_LDT	LDT_RXD3	LDT_RXD2	LDT_RXD2#	LDT_RXD5#				GND	GND	GND
M	LDT_RXD3#	LDT_RXD8	LDT_RXD6	LDT_RXD6#	LDT_TXD8#				GND	GND	GND
N	LDT_RXD8#	LDT_RXD7	LDT_RXD7#	GND	LDT_TXD8				VDD	GND	GND
P	GND	LDT_TXD7	LDT_TXD7#	LDT_TXD3	LDT_TXD3				VDD	VDD	GND
R	LDT_TXD2#	LDT_TXD2	LDT_TXD6#	LDT_TXD6	LDT_TXD5#						
T	LDT_TXCK#	LDT_TXCK	LDT_TXD4#	GND	LDT_TXD5						
U	VDD_LDT	LDT_TXD1#	LDT_TXD4	GND	VDD						
V	LDT_TXD1	LDT_TXD0#	VDD	VDD	GND	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD25	PCI_AD21	PCI_AD18
W	LDT_TXD0	VDD	PRDY#	TEST	GND	VDD_3P3	VDD_3P3	PCI_AD28	PCI_AD24	GND	PCI_AD17
Y	VDD	BUF_14M	DDC_CLK	VTT_VREF	PCI_INTB#	PCI_GNT4#	PCI_GNT3#	PCI_AD27	PCI_CBE3#	PCI_AD20	PCI_AD16
AA	GND	VDD_3P3	DDC_DATA	PCI_INTA#	PCI_INTD#	PCI_REQ4#	PCI_REQ3#	PCI_AD26	PCI_AD23	PCI_AD19	PCI_CBE2#
AB	CPU_RST#	APIC_CLK	PCI_INTE#	VDD_5	PCI_INTC#	PCI_CLK4	GND	PCI_CLK3	PCI_AD22	VDD_3P3	PCI_FRAME#

12	13	14	15	16	17	18	19	20	21	22	
IDE_ADDR_P1	GND	IDE_DATA_P0	IDE_DATA_P3	VDD_5	IDE_DATA_P7	IDE_DATA_P8	VDD_AUX3	USB_P2	USB_VDD	USB_VREF	A
IDE_ADDR_P2	IDE_RDY_P	IDE_DRQ_P	IDE_DATA_P13	IDE_DATA_P11	IDE_DATA_P6	USB_P0	USB_P1	USB_N2	VDD_USB	GND	B
IDE_DATA_P0	IDE_IOR_P#	IDE_DATA_P15	IDE_DATA_P2	IDE_DATA_P5	IDE_DATA_P9	USB_N0	USB_N1	USB_OC2	USB_N3	USB_P3	C
IDE_DACK_P#	VDD_3P3	IDE_DATA_P14	IDE_DATA_P4	GND	GND	GND	GND	USB_OC3	USB_P4	VDD_AUX3	D
IDE_INTR_P	IDE_IOW_P#	IDE_DATA_P1	IDE_DATA_P12	IDE_DATA_P10	USB_OC0	GND	GND	USB_OC4	USB_N4	USB_P5	E
						USB_OC1	GND	USB_OC5	USB_N5	SLP_S3#	F
						FANCTL0	GND	FANRPM	A20GATE	VDD_AUX3	G
						FANCTL1	LDT_RST#	PWRGD_SB	SLP_S1#	PWRGD	H
GND	VDD	VDD				EXT_SMI#	BUF_24M	THERM#	SLPBTN#	PWRBTN#	J
GND	GND	VDD				SLP_S5#	GND	KBRDRSTIN#	RI#	PME#	K
GND	GND	GND				SERIRQ#	LPC_AD0	SPDIF	SPKR	VDD_3P3	L
GND	GND	GND				LPC_DRQ0#	LPC_AD1	LPC_AD2	LPC_FRAME#	PCI_CLK6	M
GND	GND	VDD				LPC_DRQ1#	GND	LPC_AD3	AC_SDATA_OUT	VDD_AUX3	N
GND	VDD	VDD				MII_CRS	MII_TXCLK	MII_TXEN	MII_TXD3	AC_RESET#	P
						MII_TXD0	MII_TXD1	MII_TXD2	MII_MDC	MII_MDIO	R
						MII_RXD1	GND	MII_RXD2	MII_RXD3	VDD_AUX5	T
						MII_RXCLK	GND	MII_RXDV	MII_RXD0	VDD_AUXC	U
PCI_IRDY#	PCI_STOP#	PCI_SERR#	PCI_AD13	PCI_AD8	PCI_AD6	GND	GND	MII_RXER	AC_SDATA_IN0	AC_BITCLK	V
PCI_TRDY#	VDD_3P3	PCI_CBE1#	PCI_AD12	GND	GND	GND	GND	MII_COL	AC_SDATA_IN1	VDD_AUX3	W
PCI_DEVSEL#	PCI_PERR#	PCI_PAR	PCI_AD11	PCI_CBE0#	PCI_AD5	PCI_GNT1#	PCI_AD1	PCI_AD0	PCI_GNT0#	AC_SYNC	Y
PCI_REQ2#	PCI_GNT2#	PCI_AD15	PCI_AD10	PCI_AD7	PCI_AD4	PCI_REQ1#	PCI_AD2	PCI_REQ0#	PCI_CLK5	RESET#	AA
PCI_CLK2	GND	PCI_AD14	PCI_AD9	VDD_3P3	PCI_AD3	PCI_CLK1	GND	PCI_CLK0	PCI_CLKFB	VDD_5	AB

6.2 MCP-1x Ball Diagram

	1	2	3	4	5	6	7	8	9	10	11
A	SMB_CLK0	SMB_DATA0	SMB_CLK1	VDD_5	TRST0	TDI0	GND	TCK0	TMS0	VDD_3P3	TDE0#
B	RTC_XO	GND	SMB_DATA1	RSVD	TRST1	TDI1	TDO0	TDO1	TCK1	TMS1	TDE1#
C	RTC_XI	VBATT	SMB_ALERT#	VDD_AUX5	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IDE_CS1_P#
D	GND	INTRUDER	VDD_AUX3	GND	GND	VDD_3P3	VDD_3P3	RSVD	RSVD	GND	IDE_CS3_P#
E	XTAL_14M_OUT	VDD_PLL	NMI	GND	GND	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
F	XTAL_14M_IN	INTR	SMI#	CPU_VTT	CPUSLP#						
G	APIC_DATA1	APIC_DATA0	INIT#	CPU_VTT	FERR#						
H	GND	LDT_RSET	STPCLK#	A20M#	IGNNE#						
J	LDT_RXD0#	LDT_RXD0	LDT_RXD4	LDT_RXD1	LDT_RXD1#				VDD	VDD	GND
K	LDT_RXCK#	LDT_RXCK	LDT_RXD4#	GND	LDT_RXD5				VDD	GND	GND
L	VDD_LDT	LDT_RXD3	LDT_RXD2	LDT_RXD2#	LDT_RXD5#				GND	GND	GND
M	LDT_RXD3#	LDT_RXD8	LDT_RXD6	LDT_RXD6#	LDT_TXD8#				GND	GND	GND
N	LDT_RXD8#	LDT_RXD7	LDT_RXD7#	GND	LDT_TXD8				VDD	GND	GND
P	GND	LDT_TXD7	LDT_TXD7#	LDT_TXD3	LDT_TXD3				VDD	VDD	GND
R	LDT_TXD2#	LDT_TXD2	LDT_TXD6#	LDT_TXD6	LDT_TXD5#						
T	LDT_TXCK#	LDT_TXCK	LDT_TXD4#	GND	LDT_TXD5						
U	VDD_LDT	LDT_TXD1#	LDT_TXD4	GND	VDD						
V	LDT_TXD1	LDT_TXD0#	VDD	VDD	GND	XBUS_A1	XBUS_A2	XBUS_A5	XBUS_A8	XBUS_A10	XBUS_A12
W	LDT_TXD0	VDD	PRDY#	TEST	GND	VDD_3P3	VDD_3P3	XBUS_A0	XBUS_DQ1	GND	XBUS_CE#
Y	VDD	BUF_14M	DDC_CLK	VTT_VREF	PCI_INTB#	RSVD	RSVD	XBUS_A4	XBUS_A7	XBUS_DQ2	XBUS_DQ3
AA	GND	VDD_3P3	DDC_DATA	PCI_INTA#	PCI_INTD#	RSVD	RSVD	XBUS_A3	XBUS_DQ0	XBUS_A9	XBUS_A11
AB	CPU_RST#	APIC_CLK	PCI_INTE#	VDD_5	PCI_INTC#	PCI_CLK4	GND	PCI_CLK3	XBUS_A6	VDD_3P3	RSVD

12	13	14	15	16	17	18	19	20	21	22	
IDE_ADDR_P1	GND	IDE_DATA_P0	IDE_DATA_P3	VDD_5	IDE_DATA_P7	IDE_DATA_P8	VDD_AUX3	USB_P2	USB_VDD	USB_VREF	A
IDE_ADDR_P2	IDE_RDY_P	IDE_DRQ_P	IDE_DATA_P13	IDE_DATA_P11	IDE_DATA_P6	USB_P0	USB_P1	USB_N2	VDD_USB	GND	B
IDE_DATA_P0	IDE_IOR_P#	IDE_DATA_P15	IDE_DATA_P2	IDE_DATA_P5	IDE_DATA_P9	USB_N0	USB_N1	USB_OC2	USB_N3	USB_P3	C
IDE_DACK_P#	VDD_3P3	IDE_DATA_P14	IDE_DATA_P4	GND	GND	GND	GND	USB_OC3	USB_P4	VDD_AUX3	D
IDE_INTR_P	IDE_IOW_P#	IDE_DATA_P1	IDE_DATA_P12	IDE_DATA_P10	USB_OC0	GND	GND	USB_OC4	USB_N4	USB_P5	E
						USB_OC1	GND	USB_OC5	USB_N5	SLP_S3#	F
						FANCTL0	GND	FANRPM	A20GATE	VDD_AUX3	G
						FANCTL1	LDT_RST#	PWRGD_SB	SLP_S1#	PWRGD	H
GND	VDD	VDD				EXT_SMI#	BUF_24M	THERM#	SLPBTN#	PWRBTN#	J
GND	GND	VDD				SLP_S5#	GND	KBRDRSTIN#	RI#	PME#	K
GND	GND	GND				SERIRQ#	LPC_AD0	SPDIF	SPKR	VDD_3P3	L
GND	GND	GND				LPC_DRQ0#	LPC_AD1	LPC_AD2	LPC_FRAME#	PCI_CLK6	M
GND	GND	VDD				LPC_DRQ1#	GND	LPC_AD3	AC_SDATA_OUT	VDD_AUX3	N
GND	VDD	VDD				MII_CRS	MII_TXCLK	MII_TXEN	MII_TXD3	AC_RESET#	P
						MII_TXD0	MII_TXD1	MII_TXD2	MII_MDC	MII_MDIO	R
						MII_RXD1	GND	MII_RXD2	MII_RXD3	VDD_AUX5	T
						MII_RXCLK	GND	MII_RXDV	MII_RXD0	VDD_AUXC	U
RSVD	RSVD	RSVD	XBUS_A17	XBUS_A19	RSVD	GND	GND	MII_RXER	AC_SDATA_IN0	AC_BITCLK	V
RSVD	VDD_3P3	XBUS_DQ5	XBUS_A16	GND	GND	GND	GND	MII_COL	AC_SDATA_IN1	VDD_AUX3	W
RSVD	RSVD	RSVD	XBUS_DQ6	XBUS_A8	XBUS_WE#	RSVD	XBUS_A22	XBUS_A23	RSVD	AC_SYNC	Y
RSVD	RSVD	XBUS_A13	XBUS_A15	XBUS_DQ7	XBUS_OE#	RSVD	XBUS_A21	RSVD	PCI_CLK5	RESET#	AA
PCI_CLK2	GND	XBUS_DQ4	XBUS_A14	VDD_3P3	XBUS_A20	PCI_CLK1	GND	PCI_CLK0	PCI_CLKFB	VDD_5	AB

6.3 Signal List (Alphabetically)

Signal	Ball #
A20GATE	G21
A20M#	H4
AC_BITCLK	V22
AC_RESET#	P22
AC_SDATA_IN0	V21
AC_SDATA_IN1	W21
AC_SDATA_OUT	N21
AC_SYNC	Y22
APIC_CLK	AB2
APIC_DATA0	G2
APIC_DATA1	G1
BUF_14M	Y2
BUF_24M	J19
CPU_RST#	AB21
CPU_VREF	Y4
CPU_VTT	F4
CPU_VTT	G4
CPUSLP#	F5
DDC_CLK	Y3
DDC_DATA	AA3
EXTSMI#	J18
FANCTL0	G18
FANCTL1	H18
FANRPM	G20
FERR#	G5
GND	A7
GND	A13
GND	B2
GND	B22
GND	D1
GND	D4
GND	D5
GND	D10
GND	D16
GND	D17
GND	D18
GND	D19
GND	E4
GND	E5
GND	E18
GND	E19
GND	F19
GND	G19
GND	H1
GND	J11
GND	J12
GND	K4
GND	K10
GND	K11

Signal	Ball #
GND	K12
GND	K13
GND	K19
GND	L9
GND	L10
GND	L11
GND	L12
GND	L13
GND	L14
GND	M9
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	N4
GND	N10
GND	N11
GND	N12
GND	N13
GND	N19
GND	P1
GND	P11
GND	P12
GND	T4
GND	T19
GND	U4
GND	U19
GND	V5
GND	V18
GND	V19
GND	W5
GND	W10
GND	W16
GND	W17
GND	W18
GND	W19
GND	AA1
GND	AB7
GND	AB13
GND	AB19
IDE_ADDR_P0	C12
IDE_ADDR_P1	A12
IDE_ADDR_P2	B12
IDE_ADDR_S0	A5
IDE_ADDR_S1	E6
IDE_ADDR_S2	B5
IDE_CS1_P#	C11
IDE_CS1_S#	C5

Signal	Ball#
IDE_CS3_P#	D11
IDE_CS3_S#	B4
IDE_DACK_P#	D12
IDE_DACK_S#	A6
IDE_DATA_P0	A14
IDE_DATA_P1	E14
IDE_DATA_P2	C15
IDE_DATA_P3	A15
IDE_DATA_P4	D15
IDE_DATA_P5	C16
IDE_DATA_P6	B17
IDE_DATA_P7	A17
IDE_DATA_P8	A18
IDE_DATA_P9	C17
IDE_DATA_P10	E16
IDE_DATA_P11	B16
IDE_DATA_P12	E15
IDE_DATA_P13	B15
IDE_DATA_P14	D14
IDE_DATA_P15	C14
IDE_DATA_S0	B8
IDE_DATA_S1	C8
IDE_DATA_S2	D8
IDE_DATA_S3	B9
IDE_DATA_S4	D9
IDE_DATA_S5	B10
IDE_DATA_S6	E10
IDE_DATA_S7	B11
IDE_DATA_S8	A11
IDE_DATA_S9	E11
IDE_DATA_S10	C10
IDE_DATA_S11	E9
IDE_DATA_S12	A9
IDE_DATA_S13	C9
IDE_DATA_S14	E8
IDE_DATA_S15	A8
IDE_DRQ_P	B14
IDE_DRQ_S	E7
IDE_INTR_P	E12
IDE_INTR_S	B6
IDE_IOR_P#	C13
IDE_IOR_S#	B7
IDE_IOW_P#	E13
IDE_IOW_S#	C7
IDE_RDY_P	B13
IDE_RDY_S	C6
IGNNE#	H5
INIT#	G3
INTR	F2

Signal	Ball #
INTRUDER#	J19
KBRDRSTIN#	K20
LDT_RSET	H2
LDT_RST#	H19
LDT_RXCLK	K2
LDT_RXCLK#	J2
LDT_RXD0	J1
LDT_RXD0#	K1
LDT_RXD1	J4
LDT_RXD1#	J5
LDT_RXD2	M1
LDT_RXD2#	N2
LDT_RXD3	M2
LDT_RXD3#	L2
LDT_RXD4	L3
LDT_RXD4#	L4
LDT_RXD5	K3
LDT_RXD5#	J3
LDT_RXD6	M3
LDT_RXD6#	M4
LDT_RXD7	K5
LDT_RXD7#	L5
LDT_RXD8	N1
LDT_RXD8#	P2
LDT_TXCLK	V1
LDT_TXCLK#	U2
LDT_TXD0	W1
LDT_TXD0#	V2
LDT_TXD1	T1
LDT_TXD1#	T2
LDT_TXD2	R1
LDT_TXD2#	R2
LDT_TXD3	R3
LDT_TXD3#	R4
LDT_TXD4	T3
LDT_TXD4#	U3
LDT_TXD5	R5
LDT_TXD5#	T5
LDT_TXD6	M5
LDT_TXD6#	N5
LDT_TXD7	P5
LDT_TXD7#	P4
LDT_TXD8	P3
LDT_TXD8#	N3
LPC_AD0	L19
LPC_AD1	M19
LPC_AD2	M20
LPC_AD3	N20
LPC_CLK	M22

Signal	Ball #
LPC_DRQ0#	M18
LPC_DRQ1#	N18
LPC_FRAME#	M21
MII_COL	W20
MII_CRS	P18
MII_MDC	R22
MII_MDIO	R21
MII_RXCLK	U18
MII_RXD0	U21
MII_RXD1	T18
MII_RXD2	T20
MII_RXD3	T21
MII_RXDV	U20
MII_RXER	V20
MII_TXCLK	P19
MII_TXD0	R18
MII_TXD1	R19
MII_TXD2	R20
MII_TXD3	P21
MII_TXEN	P20
NMI	E3
PCI_AD0	Y20
PCI_AD1	Y19
PCI_AD2	AA19
PCI_AD3	AB17
PCI_AD4	AA17
PCI_AD5	Y17
PCI_AD6	V17
PCI_AD7	AA16
PCI_AD8	V16
PCI_AD9	AB15
PCI_AD10	AA15
PCI_AD11	Y15
PCI_AD12	W15
PCI_AD13	V15
PCI_AD14	AB14
PCI_AD15	AA14
PCI_AD16	Y11
PCI_AD17	W11
PCI_AD18	V11
PCI_AD19	AA10
PCI_AD20	Y10
PCI_AD21	V10
PCI_AD22	AB9
PCI_AD23	AA9
PCI_AD24	W9
PCI_AD25	V9
PCI_AD26	AA8
PCI_AD27	Y8

Signal	Ball#
PCI_AD28	W8
PCI_AD29	V8
PCI_AD30	V7
PCI_AD31	V6
PCI_CBE0#	Y16
PCI_CBE1#	W14
PCI_CBE2#	AA11
PCI_CBE3#	Y9
PCI_CLK0	AB20
PCI_CLK1	AB18
PCI_CLK2	AB12
PCI_CLK3	AB8
PCI_CLK4	AB6
PCI_CLK5	AA21
PCI_CLKFB	AB21
PCI_DEVSEL#	Y12
PCI_FRAME#	AB11
PCI_GNT0#	Y21
PCI_GNT1#	Y18
PCI_GNT2#	AA13
PCI_GNT3#	Y7
PCI_GNT4#	Y6
PCI_INTA#	AA4
PCI_INTB#	Y5
PCI_INTC#	AB5
PCI_INTD#	AA5
PCI_INTE#	AB3
PCI_IRDY#	V12
PCI_PAR	Y14
PCI_PERR#	Y13
PCI_REQ0#	AA20
PCI_REQ1#	AA18
PCI_REQ2#	AA12
PCI_REQ3#	AA7
PCI_REQ4#	AA6
PCI_RESET#	AA22
PCI_SERR#	V14
PCI_STOP#	V13
PCI_TRDY#	W12
PME#	K22
PRDY#	W3
PWRBTN#	J22
PWRGD	H22
PWRGD_SB	H20
RI#	K21
RTC_XI	C1
RTC_XO	B1
SERIRQ#	L18
SLP_S1#	H21

Signal	Ball #
SLP_S3#	F22
SLP_S5#	K18
SLPBTN#	J21
SMB_ALERT#	C3
SMB_CLK0	A1
SMB_CLK1	A3
SMB_DATA0	A2
SMB_DATA1	B3
SMI#	F3
SPDIF	L20
SPKR	L21
STPCLK#	H3
TEST	W4
THERM#	J20
USB_N0	C18
USB_N1	C19
USB_N2	B20
USB_N3	C21
USB_N4	E21
USB_N5	F21
USB_OC0#	E17
USB_OC1#	F18
USB_OC2#	C20
USB_OC3#	D20
USB_OC4#	E20
USB_OC5#	F20
USB_P0	B18
USB_P1	B19
USB_P2	A20
USB_P3	C22
USB_P4	D21
USB_P5	E22
USB_VREF	A22
VAUX3PLL	E2
VDD_AUXC	U22
VBATT	C2
VDD	J9
VDD	J10
VDD	J13
VDD	J14
VDD	K9
VDD	K14
VDD	N9
VDD	N14
VDD	P9
VDD	P10
VDD	P13
VDD	P14
VDD	U5

Signal	Ball #
VDD	V3
VDD	V4
VDD	W2
VDD	Y1
VDD_3P3	A10
VDD_3P3	D6
VDD_3P3	D7
VDD_3P3	D13
VDD_3P3	L22
VDD_3P3	W6
VDD_3P3	W7
VDD_3P3	W13
VDD_3P3	AA2
VDD_3P3	AB10
VDD_3P3	AB16
VDD_5	A4
VDD_5	A16
VDD_5	AB4
VDD_5	AB22
VDD_AUX3	A19
VDD_AUX3	D3
VDD_AUX3	D22
VDD_AUX3	G22
VDD_AUX3	N22
VDD_AUX3	W22
VDD_AUX5	C4
VDD_AUX5	T22
VDD_LDT	L1
VDD_LDT	U1
VDD_USB	A21
VDD_USB	B21
XTAL_14M_IN	D2
XTAL_14M_OUT	E1

6.4 Signal List (by Function)

North – South Link	
Signal	**Ball #**
LDT_RSET	H2
LDT_RST#	H19
LDT_RXCLK	K2
LDT_RXCLK#	K1
LDT_RXD0	J2
LDT_RXD0#	J1
LDT_RXD1	J4
LDT_RXD1#	J5
LDT_RXD2	L3
LDT_RXD2#	L4
LDT_RXD3	L2
LDT_RXD3#	M1
LDT_RXD4	J3
LDT_RXD4#	K3
LDT_RXD5	K5
LDT_RXD5#	L5
LDT_RXD6	M3
LDT_RXD6#	M4
LDT_RXD7	N2
LDT_RXD7#	N3
LDT_RXD8	M2
LDT_RXD8#	N1
LDT_TXCLK	T2
LDT_TXCLK#	T1
LDT_TXD0	W1
LDT_TXD0#	V2
LDT_TXD1	V1
LDT_TXD1#	U2
LDT_TXD2	R2
LDT_TXD2#	R1
LDT_TXD3	P4
LDT_TXD3#	P5
LDT_TXD4	U3
LDT_TXD4#	T3
LDT_TXD5	T5
LDT_TXD5#	R5
LDT_TXD6	R4
LDT_TXD6#	R3
LDT_TXD7	P2
LDT_TXD7#	P3
LDT_TXD8	N5
LDT_TXD8#	M5

PCI Bus Interface	
Signal	**Ball #**
PCI_AD0	Y20
PCI_AD1	Y19
PCI_AD2	AA19
PCI_AD3	AB17
PCI_AD4	AA17
PCI_AD5	Y17
PCI_AD6	V17
PCI_AD7	AA16
PCI_AD8	V16
PCI_AD9	AB15
PCI_AD10	AA15
PCI_AD11	Y15
PCI_AD12	W15
PCI_AD13	V15
PCI_AD14	AB14
PCI_AD15	AA14
PCI_AD16	Y11
PCI_AD17	W11
PCI_AD18	V11
PCI_AD19	AA10
PCI_AD20	Y10
PCI_AD21	V10
PCI_AD22	AB9
PCI_AD23	AA9
PCI_AD24	W9
PCI_AD25	V9
PCI_AD26	AA8
PCI_AD27	Y8
PCI_AD28	W8
PCI_AD29	V8
PCI_AD30	V7
PCI_AD31	V6
PCI_CBE0#	Y16
PCI_CBE1#	W14
PCI_CBE2#	AA11
PCI_CBE3#	Y9
PCI_CLK0	AB20
PCI_CLK1	AB18
PCI_CLK2	AB12
PCI_CLK3	AB8
PCI_CLK4	AB6
PCI_CLK5	AA21
PCI_CLKFB	AB21
PCI_DEVSEL#	Y12
PCI_FRAME#	AB11
PCI_GNT0#	Y21
PCI_GNT1#	T18

PCI Bus Interface	
Signal	**Ball #**
PCI_GNT2#	AA13
PCI_GNT3#	Y7
PCI_GNT4#	Y6
PCI_INTA#	AA4
PCI_INTB#	Y5
PCI_INTC#	AB5
PCI_INTD#	AA5
PCI_INTE#	AB3
PCI_IRDY#	V12
PCI_PAR	Y14
PCI_PERR#	Y13
PCI_REQ0#	AA20
PCI_REQ1#	AA18
PCI_REQ2#	AA12
PCI_REQ3#	AA7
PCI_REQ4#	AA6
PCI_RESET#	AA22
PCI_SERR#	V14
PCI_STOP#	V13
PCI_TRDY#	W12

MAC Interface	
Signal	**Ball #**
MII_COL	W20
MII_CRS	P18
MII_MDC	R21
MII_MDIO	R22
MII_RXCLK	U18
MII_RXD0	U21
MII_RXD1	T18
MII_RXD2	T20
MII_RXD3	T21
MII_RXDV	U20
MII_RXER	V20
MII_TXCLK	P19
MII_TXD0	R18
MII_TXD1	R19
MII_TXD2	R20
MII_TXD3	P21
MII_TXEN	P20

Primary IDE Interface	
Signal	**Ball #**
IDE_ADDR_P0	C12
IDE_ADDR_P1	A12
IDE_ADDR_P2	B12
IDE_CS1_P#	C11
IDE_CS3_P#	D11
IDE_DACK_P#	D12
IDE_DATA_P0	A14
IDE_DATA_P1	E14
IDE_DATA_P2	C15
IDE_DATA_P3	A15
IDE_DATA_P4	D15
IDE_DATA_P5	C16
IDE_DATA_P6	B17
IDE_DATA_P7	A17
IDE_DATA_P8	A18
IDE_DATA_P9	C17
IDE_DATA_P10	E16
IDE_DATA_P11	B16
IDE_DATA_P12	E15
IDE_DATA_P13	B15
IDE_DATA_P14	D14
IDE_DATA_P15	C14
IDE_DRQ_P	B14
IDE_INTR_P	E12
IDE_IOR_P#	C13
IDE_IOW_P#	E13
IDE_RDY_P	B13

Secondary IDE Interface	
Signal	**Ball #**
IDE_ADDR_S0	A5
IDE_ADDR_S1	E6
IDE_ADDR_S2	B5
IDE_CS1_S#	C5
IDE_CS3_S#	B4
IDE_DACK_S#	A6
IDE_DATA_S0	B8
IDE_DATA_S1	C8
IDE_DATA_S2	D8
IDE_DATA_S3	B9
IDE_DATA_S4	D9
IDE_DATA_S5	B10
IDE_DATA_S6	E10
IDE_DATA_S7	B11
IDE_DATA_S8	A11
IDE_DATA_S9	E11
IDE_DATA_S10	C10
IDE_DATA_S11	E9
IDE_DATA_S12	L9
IDE_DATA_S13	C9
IDE_DATA_S14	E8
IDE_DATA_S15	A8
IDE_DRQ_S	E7
IDE_INTR_S	B6
IDE_IOR_S#	B7
IDE_IOW_S#	C7
IDE_RDY_S	C6

CPU Interface	
Signal	**Ball #**
A20GATE	G21
A20M#	H4
APIC_CLK	AB2
APIC_DATA0	G2
APIC_DATA1	G1
CPU_RST#	AB1
VTT_VREF	Y4
FERR#	G5
IGNNE#	H5
INIT#	G3
INTR	F2
NMI	E3
SMI#	F3
STPCLK#	H3

LPC Interface	
Signal	**Ball #**
LPC_AD0	L19
LPC_AD1	M19
LPC_AD2	M20
LPC_AD3	N20
LPC_CLK	M22
LPC_DRQ0#	M18
LPC_DRQ1#	N18
LPC_FRAME#	M21
SERIRQ#	L18

Power Management	
Signal	**Ball #**
CPUSLP#	F5
EXTSMI#	J18
FANCTL0	G18
FANCTL1	H18
FANRPM	G20
INTRUDER#	D2
KBRDRSTIN#	K20
PME#	K22
PRDY#	W3
PWRBTN#	J22
PWRGD	H22
PWRGD_SB	H20
RI#	K21
SLP_S1#	H21
SLP_S3#	F22
SLP_S5#	K18
SLPBTN#	J21
THERM#	J20

AC '97 Interface	
Signal	**Ball #**
AC_BITCLK	V22
AC_RESET#	P22
AC_SDATA_OUT	N21
AC_SDATA_IN0	V21
AC_SDATA_IN1	W21
AC_SYNC	Y22

SMBus Interface	
Signal	**Ball #**
SMB_ALERT#	C3
SMB_CLK0	A1
SMB_CLK1	A3
SMB_DATA0	A2
SMB_DATA1	B3

USB Interface	
Signal	**Ball #**
USB_N0	C18
USB_N1	C19
USB_N2	B20
USB_N3	C21
USB_N4	E21
USB_N5	F21
USB_P0	B18
USB_P1	B19
USB_P2	A20
USB_P3	C22
USB_P4	D21
USB_P5	E22
USB_OC0#	E17
USB_OC1#	F18
USB_OC2#	C20
USB_OC3#	D20
USB_OC4#	E20
USB_OC5#	F20
USB_VREF	A22

Clocks	
Signal	**Ball #**
BUF_14M	Y2
BUF_24M	J19
RTC_XI	C1
RTC_XO	B1
XTAL_14M_IN	F1
XTAL_14M_OUT	E1

DDC Interface	
Signal	**Ball #**
DDC_CLK	Y3
DDC_DATA	AA3

Miscellaneous	
Signal	**Ball #**
SPDIF	L20
SPKR	L21
TEST	W4

Power	
Signal	**Ball #**
CPU_VTT	F4
CPU_VTT	G4
VDD_PLL	E2
VDD_AUXC	U22
VBATT	C2
VDD	J9
VDD	J10
VDD	J13
VDD	J14
VDD	K9
VDD	K14
VDD	N9
VDD	N14
VDD	P9
VDD	P10
VDD	P13
VDD	P14
VDD	U5
VDD	V3
VDD	V4
VDD	W2
VDD	Y1
VDD_3P3	A10
VDD_3P3	D6
VDD_3P3	D7
VDD_3P3	D13
VDD_3P3	L22
VDD_3P3	W6

Power	
Signal	**Ball #**
VDD_3P3	W7
VDD_3P3	W13
VDD_3P3	AA2
VDD_3P3	AB10
VDD_3P3	AB16
VDD_AUX3	A19
VDD_AUX3	D3
VDD_AUX3	D22
VDD_AUX3	G22
VDD_AUX3	N22
VDD_AUX3	W22
VDD_AUX5	C4
VDD_AUX5	T22
VDD_5	A4
VDD_5	A16
VDD_5	AB4
VDD_5	AB22
VDD_LDT	L1
VDD_LDT	U1
VDD_USB	A21
VDD_USB	B21

Ground	
Signal	**Ball #**
GND	A7
GND	A13
GND	B2
GND	B22
GND	D1
GND	D4
GND	D5
GND	D10
GND	D16
GND	D17
GND	D18
GND	D19
GND	E4
GND	E5
GND	E18
GND	E19
GND	F19
GND	G19
GND	H1
GND	J11
GND	J12
GND	K4
GND	K10

Ground	
Signal	**Ball #**
GND	K11
GND	K12
GND	K13
GND	K19
GND	L9
GND	L10
GND	L11
GND	L12
GND	L13
GND	L14
GND	M9
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	N4
GND	N10
GND	N11
GND	N12
GND	N13
GND	N19
GND	P1
GND	P11
GND	P12
GND	T4
GND	T19
GND	U4
GND	U19
GND	V5
GND	V18
GND	V19
GND	W5
GND	W10
GND	W16
GND	W17
GND	W18
GND	W19
GND	AA1
GND	AB7
GND	AB13
GND	AB19

6.5 Signal List (Numerically – Balls)

Ball #	Signal
A1	SMB_CLK0
A2	SMB_DATA0
A3	SMB_CLK1
A4	VDD_5
A5	IDE_ADDR_S0
A6	IDE_DACK_S#
A7	GND
A8	IDE_DATA_S15
A9	IDE_DATA_S12
A10	VDD_3P3
A11	IDE_DATA_S8
A12	IDE_ADDR_P1
A13	GND
A14	IDE_DATA_P0
A15	IDE_DATA_P3
A16	VDD_5
A17	IDE_DATA_P7
A18	IDE_DATA_P8
A19	VDD_AUX3
A20	USB_P2
A21	VDD_USB
A22	USB_VREF

Ball #	Signal
B1	RTC_XO
B2	GND
B3	SMB_DATA1
B4	IDE_CS3_S#
B5	IDE_ADDR_S2
B6	IDE_INTR_S
B7	IDE_IOR_S#
B8	IDE_DATA_S0
B9	IDE_DATA_S3
B10	IDE_DATA_S5
B11	IDE_DATA_S7
B12	IDE_ADDR_P2
B13	IDE_RDY_P
B14	IDE_DRQ_P
B15	IDE_DATA_P13
B16	IDE_DATA_P11
B17	IDE_DATA_P6
B18	USB_P0
B19	USB_P1
B20	USB_N2
B21	VDD_USB
B22	GND

Ball #	Signal
C1	RTC_XI
C2	VBATT
C3	SMB_ALERT#
C4	VDD_AUX5
C5	IDE_CS1_S#
C6	IDE_RDY_S
C7	IDE_IOW_S#
C8	IDE_DATA_S1
C9	IDE_DATA_S13
C10	IDE_DATA_S10
C11	IDE_CS1_P#
C12	IDE_ADDR_P0
C13	IDE_IOR_P#
C14	IDE_DATA_P15
C15	IDE_DATA_P2
C16	IDE_DATA_P5
C17	IDE_DATA_P9
C18	USB_N0
C19	USB_N1
C20	USB_OC2
C21	USB_N3
C22	USB_P3

Ball #	Signal
D1	GND
D2	INTRUDER
D3	VDD_AUX3
D4	GND
D5	GND
D6	VDD_3P3
D7	VDD_3P3
D8	IDE_DATA_S2
D9	IDE_DATA_S4
D10	GND
D11	IDE_CS3_P#
D12	IDE_DACK_P#
D13	VDD_3P3
D14	IDE_DATA_P14
D15	IDE_DATA_P4
D16	GND
D17	GND
D18	GND
D19	GND
D20	USB_OC3
D21	USB_P4
D22	VDD_AUX3

Ball #	Signal
E1	XTAL_14M_OUT
E2	VDD_PLL
E3	NMI
E4	GND
E5	GND
E6	IDE_ADDR_S1
E7	IDE_DRQ_S
E8	IDE_ADDR_S14
E9	IDE_DATA_S11
E10	IDE_DATA_S6
E11	IDE_DATA_S9
E12	IDE_INTR_P
E13	IDE_IOW_P#
E14	IDE_DATA_P1
E15	IDE_DATA_P12
E16	IDE_DATA_P10
E17	USB_OC0
E18	GND
E19	GND
E20	USB_OC4
E21	USB_N4
E22	USB_P5

Ball #	Signal
F1	XTAL_14M_IN
F2	INTR
F3	SMI#
F4	CPU_VTT
F5	CPUSLP#
F6	-
F7	-
F8	-
F9	-
F10	-
F11	-
F12	-
F13	-
F14	-
F15	-
F16	-
F17	-
F18	USB_OC1
F19	GND
F20	USB_OC5
F21	USB_N5
F22	SLP_S3#

Ball #	Signal
G1	APIC_DATA1
G2	APIC_DATA0
G3	INIT#
G4	CPU_VTT
G5	FERR#
G6	-
G7	-
G8	-
G9	-
G10	-
G11	-
G12	-
G13	-
G14	-
G15	-
G16	-
G17	-
G18	FANCTL0
G19	GND
G20	FANRPM
G21	A20GATE
G22	VDD_AUX3

Ball #	Signal
H1	GND
H2	LDT_RSET
H3	STPCLK#
H4	A20M#
H5	IGNNE#
H6	-
H7	-
H8	-
H9	-
H10	-
H11	-
H12	-
H13	-
H14	-
H15	-
H16	-
H17	-
H18	FANCTL1
H19	LDT_RST#
H20	PWRGD_SB
H21	SLP_S1#
H22	PWRGD

Ball #	Signal
J1	LDT_RXD0#
J2	LDT_RXD0
J3	LDT_RXD4
J4	LDT_RXD1
J5	LDT_RXD1#
J6	-
J7	-
J8	-
J9	VDD
J10	VDD
J11	GND
J12	GND
J13	VDD
J14	VDD
J15	-
J16	-
J17	-
J18	EXT_SMI#
J19	BUF_24M
J20	THERM#
J21	SLTBTN#
J22	PWBTN#

Ball #	Signal
K1	LDT_RXCK#
K2	LDT_RXCK
K3	LDT_RXD4#
K4	GND
K5	LDT_RXD5
K6	-
K7	-
K8	-
K9	VDD
K10	GND
K11	GND
K12	GND
K13	GND
K14	VDD
K15	-
K16	-
K17	-
K18	SLP_S5#
K19	GND
K20	KBRDRSTIN#
K21	RI#
K22	PME#

Ball #	Signal
L1	VDD_LDT
L2	LDT_RXD3
L3	LDT_RXD2
L4	LDT_RXD2#
L5	LDT_RXD5#
L6	-
L7	-
L8	-
L9	GND
L10	GND
L11	GND
L12	GND
L13	GND
L14	GND
L15	-
L16	-
L17	-
L18	SERIRQ#
L19	LPC_AD0
L20	SPDIF
L21	SPKR
L22	VDD_3P3

Ball #	Signal
M1	LDT_RXD3#
M2	LDT_RXD8
M3	LDT_RXD6
M4	LDT_RXD6#
M5	LDT_TXD8#
M6	-
M7	-
M8	-
M9	GND
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	-
M16	-
M17	-
M18	LPC_DRQ0#
M19	LPC_AD1
M20	LPC_AD2
M21	LPC_FRAME#
M22	LPC_CLK

Ball #	Signal
N1	LDT_RXD8#
N2	LDT_RXD7
N3	LDT_RXD7#
N4	GND
N5	LDT_TXD8
N6	-
N7	-
N8	-
N9	VDD
N10	GND
N11	GND
N12	GND
N13	GND
N14	VDD
N15	-
N16	-
N17	-
N18	LPC_DRQ1#
N19	GND
N20	LPC_AD3
N21	AC_SDATA_OUT
N22	VDD_AUX3

Ball #	Signal
P1	GND
P2	LDT_TXD7
P3	LDT_TXD7#
P4	LDT_TXD3
P5	LDT_TXD3#
P6	-
P7	-
P8	-
P9	VDD
P10	VDD
P11	GND
P12	GND
P13	VDD
P14	VDD
P15	-
P16	-
P17	-
P18	MII_CRS
P19	MII_TXCLK
P20	MII_TXEN
P21	MII_TXD3
P22	AC_RESET#

Ball #	Signal
R1	LDT_TXD2#
R2	LDT_TXD2
R3	LDT_TXD6#
R4	LDT_TXD6
R5	LDT_TXD5#
R6	-
R7	-
R8	-
R9	-
R10	-
R11	-
R12	-
R13	-
R14	-
R15	-
R16	-
R17	-
R18	MII_TXD0
R19	MII_TXD1
R20	MII_TXD2
R21	MII_MDC
R22	MII_MDIO

Ball #	Signal
T1	LDT_TXCK#
T2	LDT_TXCK
T3	LDT_TXD4#
T4	GND
T5	LDT_TXD5
T6	-
T7	-
T8	-
T9	-
T10	-
T11	-
T12	-
T13	-
T14	-
T15	-
T16	-
T17	-
T18	MII_RXD1
T19	GND
T20	MII_RXD2
T21	MII_RXD3
T22	VDD_AUX5

Ball #	Signal
U1	VDD_LDT
U2	LDT_TXD1#
U3	LDT_TXD4
U4	GND
U5	VDD
U6	-
U7	-
U8	-
U9	-
U10	-
U11	-
U12	-
U13	-
U14	-
U15	-
U16	-
U17	-
U18	MII_RXCLK
U19	GND
U20	MII_RXDV
U21	MII_RXD0
U22	VDD_AUXC

Ball #	Signal
V1	LDT_TXD1
V2	LDT_TXD0#
V3	VDD
V4	VDD
V5	GND
V6	PCI_AD31
V7	PCI_AD30
V8	PCI_AD29
V9	PCI_AD25
V10	PCI_AD21
V11	PCI_AD18
V12	PCI_IRDY#
V13	PCI_STOP#
V14	PCI_SERR#
V15	PCI_AD13
V16	PCI_AD8
V17	PCI_AD6
V18	GND
V19	GND
V20	MII_RXER
V21	AC_SDATA_IN0
V22	AC_BITCLK

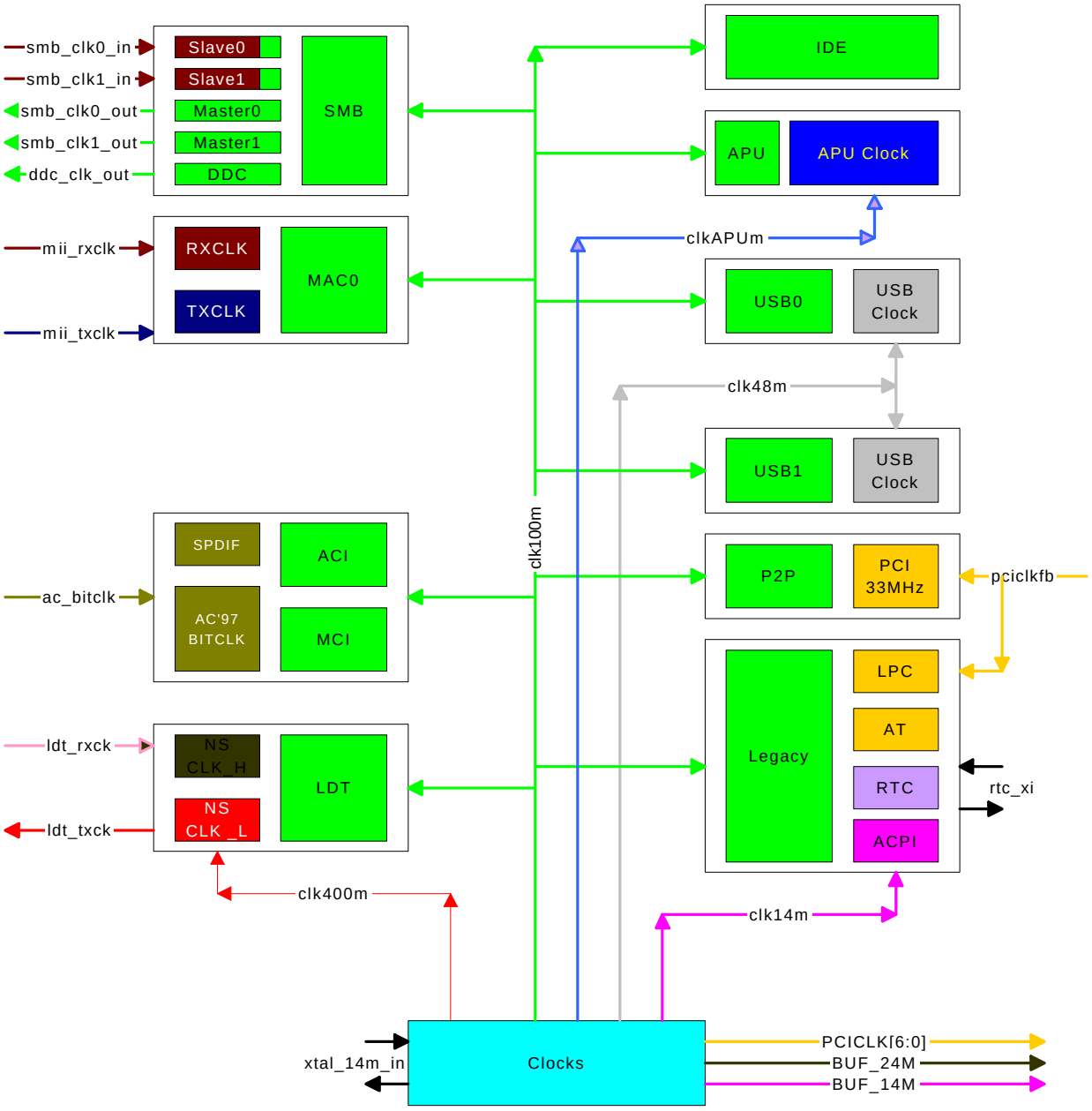
Ball #	Signal
W1	LDT_TXD0
W2	VDD
W3	PRDY#
W4	TEST
W5	GND
W6	VDD_3P3
W7	VDD_3P3
W8	PCI_AD28
W9	PCI_AD24
W10	GND
W11	PCI_AD17
W12	PCI_TRDY#
W13	VDD_3P3
W14	PCI_CBE1#
W15	PCI_AD12
W16	GND
W17	GND
W18	GND
W19	GND
W20	MII_COL
W21	AC_SDATA_IN1
W22	VDD_AUX3

Ball #	Signal
Y1	VDD
Y2	BUF_14M
Y3	DDC_CLK
Y4	VTT_VREF
Y5	PCI_INTB#
Y6	PCI_GNT4#
Y7	PCI_GNT3#
Y8	PCI_AD27
Y9	PCI_CBE3#
Y10	PCI_AD20
Y11	PCI_AD16
Y12	PCI_DEVSEL#
Y13	PCI_PERR#
Y14	PCI_PAR
Y15	PCI_AD11
Y16	PCI_CBE0#
Y17	PCI_AD5
Y18	PCI_GNT1#
Y19	PCI_AD1
Y20	PCI_AD0
Y21	PCI_GNT0#
Y22	AC_SYNC

Ball #	Signal
AA1	GND
AA2	VDD_3P3
AA3	DDC_DATA
AA4	PCI_INTA#
AA5	PCI_INTD#
AA6	PCI_REQ4#
AA7	PCI_REQ3#
AA8	PCI_AD26
AA9	PCI_AD23
AA10	PCI_AD19
AA11	PCI_CBE2#
AA12	PCI_REQ2#
AA13	PCI_GNT2#
AA14	PCI_AD15
AA15	PCI_AD10
AA16	PCI_AD7
AA17	PCI_AD4
AA18	PCI_REQ1#
AA19	PCI_AD2
AA20	PCI_REQ0#
AA21	PCI_CLK5
AA22	PCI_RESET#

Ball #	Signal
AB1	CPU_RST#
AB2	APIC_CLK
AB3	PCI_INTE#
AB4	VDD_5
AB5	PCI_INTC#
AB6	PCK_CLK4
AB7	GND
AB8	PCI_CLK3
AB9	PCK_AD22
AB10	VDD_3P3
AB11	PCI_FRAME#
AB12	PCI_CLK2
AB13	GND
AB14	PCI_AD14
AB15	PCI_AD9
AB16	VDD_3P3
AB17	PCI_AD3
AB18	PCI_CLK1
AB19	GND
AB20	PCI_CLK0
AB21	PCI_CLKFB
AB22	VDD_5

7.0 MCP Clocking



8.0 XMode Operation

XMode is a Microsoft specific feature that can only be enabled via internal bond pads.

8.1 Bonding Options

MCP1 uses the following Bonding Options:

Pin Strap	Function	Bonded Value
XBox Mode[1:0]	XBox Functionality	00 – PC-Mode 01 – X-Mode; PCI Bus; Internal ROM Disabled 10 – X-Mode; ROM Bus; Internal ROM Disabled; 11 – X-Mode; ROM Bus; Internal ROM Enabled;

The bond pads are powered off of the VDD3 ring.

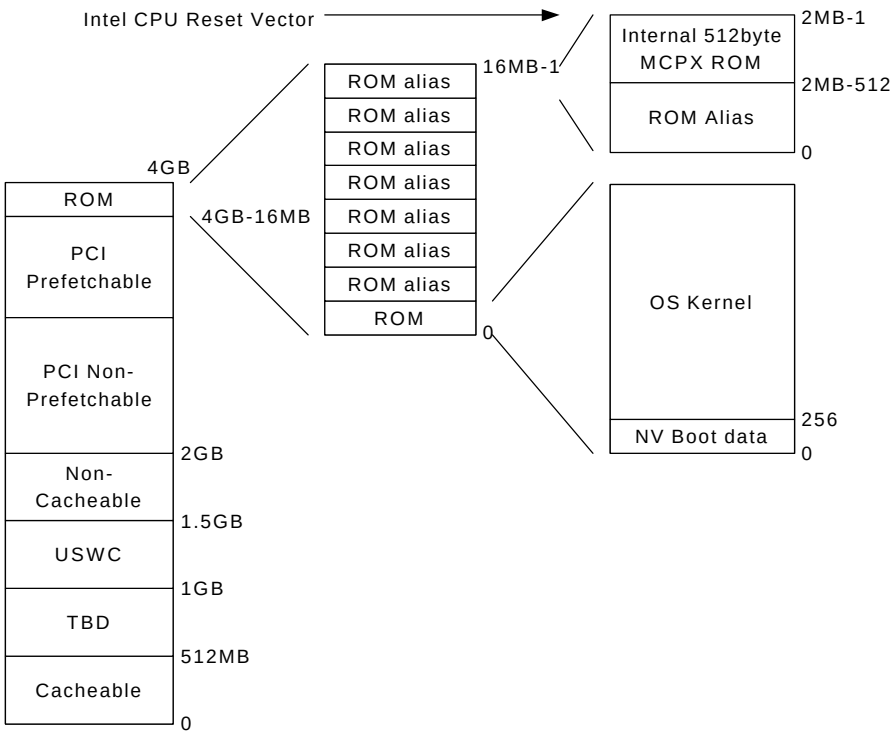
Note: Xbox Mode[0] is available as a pin during the prototyping stage.

8.2 XMode Addressing

MCP1 can operate in two modes: PC-Mode and X-Mode. While in PC-Mode, all standard AT functionality and addressing modes are supported. X-Mode has this additional functionality:

1) PCI Bus Pins can be used as parallel ROM Bus. Two ROM speeds are supported. The ROM is addressed as below.
2) The top 512 bytes of ROM can be accessed via an internal ROM or an external ROM.
3) The interrupt controller allows the 8254 Timer 1 and Timer 2 to be used as interrupts.

X-Mode Address Map



The X-Mode address map causes no changes to the MCP1 hardware except for when the ROM Bus is active. When the ROM Bus is active the ROM space is positively decoded to use this ROM.

8.3 XBox ROM Addressing

The ROM will sit at the top of the 32-bit address space. It can be up to 16MB in size. Smaller ROMs are aliased.

FF00_0000 – FFFF_FFFF	ROM Bus – 16MB
0000_0000 – FEFF_FFFF	System Address Space: Device Space System Memory

If the ROM Bus is not active, the ROM cycles will go to the LPC bus. The MCP will read the first Dword of ROM space via the ROM Bus to determine if the device exists on this bus or not. The LS bit[0] will be driven high if the ROM is present. A pull-down will be used on the system board to pull it low if the ROM is not present. The rest of the lines are don't cares.

Data read from 0xFF00_0000	Result
xxxx_xxx0	ROM is on LPC Bus – Send all ROM cycles to LPC bus.
xxxx_xxx1	ROM is on ROM Bus – Continue cycles on this bus.

The top 512 bytes are typically contained inside the MCP device, as determined by the bond option. This is a secure code space which allows an encrypted ROM to be supported. Pre-production devices will allow this space to be located outside of the device for debug and development. These top 512 bytes will not be aliased in lower address spaces if the ROM is smaller than 16MB, therefore this ROM location can be accessed in one of these aliases.

FFFF_FE00 – FFFF_FFFF	Internal ROM
FF00_0000 – FFFD_FFFF	External ROM

8.4 Boot Settings

Boot setting will be stored in the ROM rather than using strapping registers in the system. The table will be the first 16 Dwords of the ROM space (Address = 0xFF00_0000 to 0xFF00_0003F). The top of this table will be used by MCP to read any boot setting it requires. The bottom of this table will be used by the NV2X to read any boot settings it requires.

Boot Setting Table

FF00_0000 + 0x3C	MCPX Setting
FF00_0000 + 0x38-0x1C	Reserved
FF00_0000 + 0x18	NV2x Setting
FF00_0000 + 0x00	NV2x Setting (Bit[0] determines which bus the ROM is on)

8.5 MCPX Pin Muxing

MCP-1 Signal Name	MCPX Signal Name
IDE_ADDR_S0	TRST0
IDE_ADDR_S1	Reserved
IDE_ADDR_S2	TRST1
IDE_CS1_S#	Reserved
IDE_CS3_S#	Reserved
IDE_DACK_S#	TDI0
IDE_DATA_S0	TDO1
IDE_DATA_S1	Reserved
IDE_DATA_S2	Reserved
IDE_DATA_S3	TCK1
IDE_DATA_S4	Reserved
IDE_DATA_S5	TMS1
IDE_DATA_S6	Reserved
IDE_DATA_S7	TDE1#
IDE_DATA_S8	TDE0#
IDE_DATA_S9	Reserved
IDE_DATA_S10	Reserved
IDE_DATA_S11	Reserved
IDE_DATA_S12	TMS0
IDE_DATA_S13	Reserved
IDE_DATA_S14	Reserved
IDE_DATA_S15	TCK0
IDE_DRQ_S	Reserved
IDE_INTR_S	TDI1
IDE_IOR_S#	TDO0
IDE_IOW_S#	Reserved
IDE_RDY_S	Reserved
PCI_GNT0#	Reserved
PCI_GNT1#	Reserved
PCI_GNT2#	Reserved
PCI_GNT3#	Reserved
PCI_GNT4#	Reserved
PCI_IRDY#	Reserved
PCI_PAR	Reserved
PCI_PERR#	Reserved
PCI_REQ0#	Reserved
PCI_REQ1#	Reserved
PCI_REQ2#	Reserved
PCI_REQ3#	Reserved
PCI_REQ4#	Reserved
PCI_SERR#	Reserved
PCI_STOP#	Reserved
PCI_TRDY#	Reserved

MCP-1 Signal Name	MCPX Signal Name
PCI_AD0	XBUS_A23
PCI_AD1	XBUS_A22
PCI_AD2	XBUS_A21
PCI_AD3	XBUS_A20
PCI_AD4	XBUS_OE#
PCI_AD5	XBUS_WE#
PCI_AD6	Reserved
PCI_AD7	XBUS_DQ7
PCI_AD8	XBUS_A19
PCI_AD9	XBUS_A14
PCI_AD10	XBUS_A15
PCI_AD11	XBUS_DQ6
PCI_AD12	XBUS_A16
PCI_AD13	XBUS_A17
PCI_AD14	XBUS_DQ4
PCI_AD15	XBUS_A13
PCI_AD16	XBUS_DQ3
PCI_AD17	XBUS_CE#
PCI_AD18	XBUS_A12
PCI_AD19	XBUS_A9
PCI_AD20	XBUS_DQ2
PCI_AD21	XBUS_A10
PCI_AD22	XBUS_A6
PCI_AD23	XBUS_DQ0
PCI_AD24	XBUS_DQ1
PCI_AD25	XBUS_A8
PCI_AD26	XBUS_A3
PCI_AD27	XBUS_A4
PCI_AD28	XBUS_A0
PCI_AD29	XBUS_A5
PCI_AD30	XBUS_A2
PCI_AD31	XBUS_A1
PCI_CBE0#	XBUS_A18
PCI_CBE1#	XBUS_DQ5
PCI_CBE2#	XBUS_A11
PCI_CBE3#	XBUS_A7
PCI_DEVSEL#	Reserved
PCI_FRAME#	Reserved

8.6 X-Mode Pin Definitions

All other pin functionality stays the same.

X-Bus ROM Interface

Signal Name(s)	Power Plane	Dir	Description
XBUS_A[23:0]	V3P3 (5V)	Out	XBUS_A [23:0] address lines are used to access the Flash memory on the ROM bus.
XBUS_DQ[7:0]	V3P3 (5V)	I/O	XBUS_DQ[7:0] provides the data path for devices residing on the ROM Bus.
XBUS_CE#	V3P3 (5V)	Out	XBUS_CE # is the Flash BIOS device select. It is active for any memory cycles decodes to its programmed range.
XBUS_OE#	V3P3 (5V)	Out	XBUS_OE # is the command to a ROM Bus memory slave device indicating that it can drive data onto the data bus.
XBUS_WE#	V3P3 (5V)	Out	XBUS_WE# is the command to a ROM Bus memory slave device indicating that it can latch data from the data bus.

X-Mode JTAG Interface

Signal Name(s)	Power Plane	Dir	Description
TRST[1:0]	V3P3 (5V)	In	TRST[1:0] provide the Test Reset for the two separate JTAG debug port for the DSPs ([0]=GP, [1]=EP).
TDI[1:0]	V3P3 (5V)	In	TDI[1:0] provide the Data In for the two separate JTAG debug port for the DSPs ([0]=GP
TDO[1:0]	V3P3 (5V)	Out	TDO[1:0] provide the Test Data Out for the two separate JTAG debug port for the DSPs ([0]=GP, [1]=EP).
TCK[1:0]	V3P3 (5V)	In	TCK [1:0] provide the Test Clock for the two separate JTAG debug port for the DSPs ([0]=GP, [1]=EP).
TMS[1:0]	V3P3 (5V)	In	TMS[1:0] provide the Test Mode Select for the two separate JTAG debug port for the DSPs ([0]=GP, [1]=EP).
TDE[1:0]	V3P3 (5V)	I/O	TDE[1:0] provide the Test Debug Event for the two separate JTAG debug port for the DSPs ([0]=GP, [1]=EP).

8.7 Addressing

8.7.1 General

All internal devices are positively decoded using the PCI BARs.

The ROM Bus is positively decoded at a fixed address of FF00_0000 to FFFF_FFFF only.

All subtractive transactions will go to the LPC Bus.

8.7.2 ROM

The ROM will sit at the top of the 32-bit address space. It can be up to 16MB in size. Smaller ROMs are aliased.

FF00_0000 – FFFF_FFFF	ROM Bus – 16MB
0000_0000 – FEFF_FFFF	System Address Space: 1) Device Space 2) System Memory

If the ROM Bus is not active, the ROM cycles will go to the LPC bus. The MCP will read the first Dword of ROM space via the ROM Bus to determine if the device exists on this bus or not. The LS bit[0] will be driven high if the ROM is present. A pull-down will be used on the system board to pull it low if the ROM is not present. The rest of the lines are don't cares.

Data read from 0xFF00_0000	Result
Bit[0] = 0	ROM is on LPC Bus – Send all ROM cycles to LPC bus.
Bit[0] = 1	ROM is on ROM Bus – Continue cycles on this bus.

The top 512 bytes are typically contained inside the MCP device. This is a secure code space which allows an encrypted ROM to be supported. Pre-production devices will allow this space to be located outside of the device for debug and development. The 512 bytes will not be aliased in lower address spaces if the ROM is smaller than 16MB, therefore this ROM location can be accessed in one of these aliases.

FFFF_FE00 – FFFF_FFFF	Internal ROM
FF00_0000 – FFFD_FFFF	External ROM

8.7.3 Boot Settings

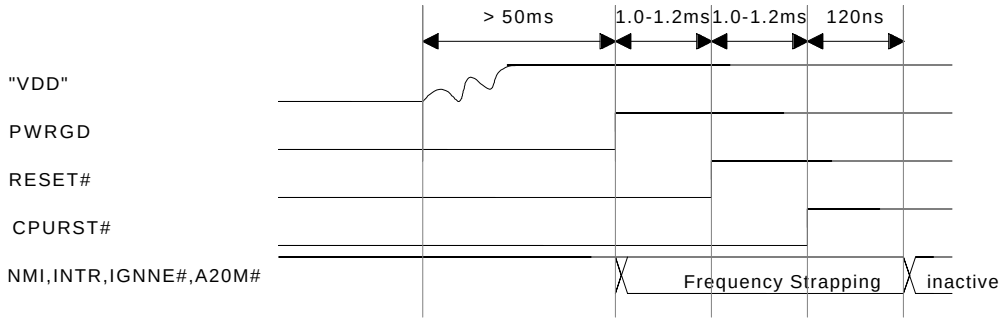
Boot setting will be stored in the ROM rather than using strapping registers in the system. The table will be the first 64 Dwords of the ROM space (Address = 0xFF00_0000 to 0xFF00_000FF). A portion of this table will be used by the NV2A and MCP to read any boot setting they require.

Boot Setting Table (256Bytes)

FF00_00FF + FF00_0080	NV2A Processor Boot Table
FF00_007F + FF00_0070	MCP Settings
FF00_006F – FF00_0004	NV2A Settings
FF00_0003 – FF00_0000	Header (0x2B16D065) If this setting is not correct the NV2A will hold the CPU in reset permanently.

8.8 Reset

The system reset is controlled by the RESET# signal. The MCP will use PWRGD to determine when to assert reset. RESET# is used to reset most of the system's peripheral logic, including the NV2A, LDT Bus, CPU, and LPC Bus.



CPURST# is used to reset the CPU and it's cache. This is driven by the NV2A and used by the MCP to correctly assert the Frequency Strapping.

PWRGD (Power Good) is driven from the power supply to signal that the VDD rail is stable. This is the main source of reset for much of the internal logic. RESET# is generated from this signal once power is stable.

INIT# is asserted for 16 PCI Clocks to reset the processor. This is generated by a combination of events. The 16-clock counter for INIT# assertion will halt while STPCLK# is active. Therefore, if INIT# is supposed to go active while STPCLK# is asserted, it will actually go active after STPCLK# is de-asserted.

Causes for INIT# or RESET# to go active:

- Shutdown special cycle from the CPU
- PORT92 bit[0] write, where the INIT_NOW transitions from a 0 to a 1.
- PORTCF9 bit[1] write, where RST_CPU bit[2] was a 0 and SYS_RST bit[1] transitions from a 0 to a 1.

BASE:Register [Bit]	Name	Description
(PORT92)0x0092 [0]	INIT_NOW	INIT Now When this bit is low and then written to a high, MCP generates a 1.0 to 1.5 microsecond pulse to either the RESET# pin or the INIT# pins, based on the state of CPURS. This bit must be written to a low again before another CPU reset can be generated.
(PORTCF9)0x0CF9[1]	SYS_RST	This bit specifies whether a full system reset with RESET# or a CPU INIT is generated when RST_CMD is written to a 1. 0 = When RST_CPU bit goes from 0 to 1, a "soft" reset is performed by activating INIT# for 480ns. 1 = When RST_CPU bit goes from 0 to 1, a "hard" reset is performed by activating RESET# for 1.5 – 2.0ms.
(PORTCF9)0x0CF9[2]	RST_CPU	A 0 to 1 transition of this bit, initiates a "hard" or "soft" reset as determined by SYS_RST.
(PORTCF9)0x0CF9[3]	FULL_RST	Full Reset. This is the same as SYS_RST for this system.

8.9 CPU Speed / Frequency Strapping

For Intel CPUs, the MCP directly sets the speed straps for the processor, saving external logic.
The MCP will perform the following:

1) While RESET# is active, the MCP drives A20M#, IGNNE#, NMI, and INTR high.
2) As soon as PWRGD goes active, the MCP read the FREQ_STRAP field contents in the ROM.

FREQ_STRAP[3:0]	Signal
[0]	NMI
[1]	INTR
[2]	IGNNE#
[3]	A20M#

The FREQ_STRAP setting are stored in the ROM settings.

9.0 Electrical Specifications (PRELIMINARY)

9.1 Absolute Maximum Ratings

Characteristic	Value
Case Temperature under Bias	0°C to 100°C
Storage Temperature	-50°C to 150°C
Voltage on any 1.5V Pin with respect to Ground	-0.5V to 1.65V
Voltage on any 3.3V Pin with respect to Ground	-0.5V to 3.6V
Voltage on any 5.0V Tolerant Pin with respect to Ground	-0.5V to 5.5V
Core 1.5V Supply Voltage	-0.5V to 1.65V
Battery 1.5V Supply Voltage	-0.5V to 1.65V
Maximum Power Dissipation	2.0W (Initial estimate)

9.2 Thermal Operation

Characteristic	Value
Thermal Operating Temperature Range (T_{CASE})	0°C to 88°C

9.3 D.C. Characteristics

V1P5 = 1.5V +0.15/- 0.05V (Max = 1.65V; Min = 1.25V)
V3P3 = 3.3V +/- 0.3V (Max = 3.6V; Min = 3.0V)
V5P0 = 5.0V +/- 0.5V (Max = 5.5V; Min = 4.5V)
T_{CASE} = 0°C to 88°C

9.3.1 D.C. Current Characteristics

Symbol	Characteristic	Min	Typical	Max	Comments
Icc Core (1.5V)	Core supply current			TBD	
Icc RTC (1.5V)	RTC supply current			TBD	
Icc Ring (1.5V)	1.5V I/O supply current			TBD	
Icc Ring (3.3V)	3.3V I/O supply current			TBD	

9.3.2 D.C. Input Characteristics

Symbol	Characteristic	Min	Typical	Max	Comments
V_{IL1P5}	Input Low Voltage (1.5V)	-0.5V		0.5V	
V_{IH1P5}	Input High Voltage (1.5V)	1.0V		1.65V	
V_{IL_IF}	Input Low Voltage (3.3V)	-0.5V		0.8V	IDE_DATA, IDE_DRQ#,

V_{IH_IF}	Input High Voltage (3.3V – 5V tolerant)	2.0V		5.5V	IDE_RDY#, IDE_INTR, MII_TXCLK, MII_RXD, MII_RXCLK, MII_RXDV, MII_RXER, MII_COL, MII_CRS, MII_MDIO, XD, CLK13P5, PWRGD, PWRGD_SB, GPIO
V_{IL_AC}	Input Low Voltage (3.3V)	-0.5V		1.0V	AC_SDATA_IN, AC_BITCLK, USB_OC
V_{IH_AC}	Input High Voltage (3.3V – 5V tolerant)	2.0V		5.5V	
V_{IL_SMB}	Input Low Voltage (3.3V)	-0.5V		0.6V	SMB_CLK, SMB_DATA, DDC_CLK, DDC_DATA
V_{IH_SMB}	Input High Voltage (3.3V – 5V tolerant)	1.4V		5.5V	
V_{IL_CPU}	Input Low Voltage (3.3V)	-0.5V		0.6V	FERR#, CPURST#, TEST#
V_{IH_CPU}	Input High Voltage (3.3V)	1.2V		3.6V	
V_{IL_USB}	Input Low Voltage (USB)	-1.0V		0.8V	USB_P, USB_N
V_{IH_USB}	Input High Voltage (USB)	2.0V		4.6V	

9.3.3 D.C. Output Characteristics

Symbol	Characteristic	Min	Typical	Max	Comments
V_{OL1P5}	Output Low Voltage (1.5V)			0.3V	
V_{OH1P5}	Output High Voltage (1.5V)	1.2V			
V_{OL_IF}	Output Low Voltage (3.3V)			0.3V	I_{OL_IF} = 4mA, I_{OH_IF} = -1mA IDE_ADDR, IDE_DATA, IDE_CS1#, IDE_CS3#, IDE_DACK#, IDE_IOR#, IDE_IOW#, MII_TXD, MII_TXEN, MII_MDC, MII_MDIO, XA, XCS#, XMEMR#, XMEMW#, GPIO
V_{OH_IF}	Output High Voltage (3.3V)	3.0V			
V_{OL_AC}	Input Low Voltage (3.3V)			0.3V	I_{OL_IF} = 4mA, I_{OH_IF} = -1mA AC_RESET#, AC_SYNC, AC_SDATA_OUT, SPDIF_OUT
V_{OH_AC}	Input High Voltage (3.3V – 5V tolerant)	3.0V			
V_{OL_SMB}	Input Low Voltage (3.3V)			0.3V	I_{OL_IF} = 4mA SMB_CLK, SMB_DATA, DDC_CLK, DDC_DATA
V_{OH_SMB}	Input High Voltage (3.3V)	Open Drain Signal: V_{OH_SMB} Controlled by Pull-Up			
V_{OL_CPU}	Output Low Voltage (3.3V)			0.6V	I_{OL_CPU} = 12mA INTR, NMI, SMI#, INIT#, A20M#, IGNNE#
V_{OH_CPU}	Output High Voltage (3.3V)	Open Drain Signal: V_{OH_CPU} Controlled by Pull-Up			
V_{OLUSB}	Output Low Voltage (USB)			0.3V	USB_P, USB_N
V_{OHUSB}	Output High Voltage (USB)	2.8V			

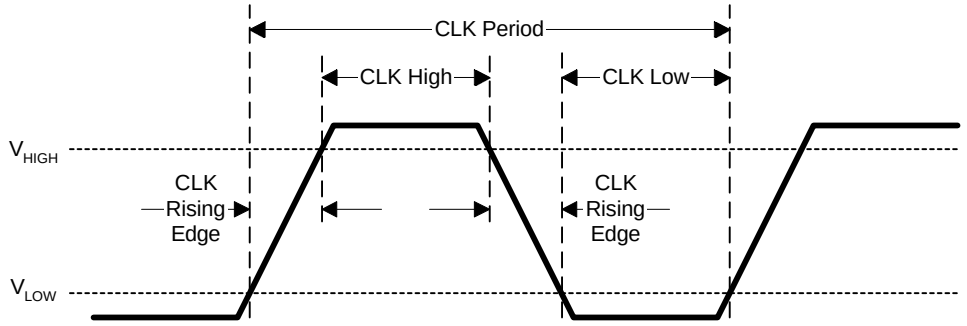
9.4 A.C. Characteristics

V1P5 = 1.5V +0.15V/- 0.05V (Max = 1.65V; Min = 1.45V)
V3P3 = 3.3V +/- 0.3V (Max = 3.6V; Min = 3.0V)
T_{CASE} = 0°C to 88°C

9.4.1 A.C. Clock Characteristics

Symbol	Characteristic	Min	Typical	Max	Comments
13.5 MHz Clock					
	CLK13P5M Frequency		13.50MHz		
	CLK13P5M Period		74.074 ns		
	CLK13P5M High Time	33.0ns		41.0ns	55/45 Duty Cycle
	CLK13P5M Low Time	33.0ns		41.0ns	55/45 Duty Cycle
	CLK13P5M Rise Time	1ns		4ns	
	CLK13P5M Fall Time	1ns		4ns	
AC'97 Clock					
	AC_BITCLK Frequency		12.288MHz		
	AC_BITCLK Period		81.38ns		
	AC_BITCLK High Time	36.0ns	40.7ns	45.0ns	55/45 Duty Cycle
	AC_BITCLK Low Time	36.0ns	40.7ns	45.0ns	55/45 Duty Cycle
	AC_BITCLK Rise Time	1ns		4ns	
	AC_BITCLK Fall Time	1ns		4ns	
MII Transmit Clock					
	MII_TXCLK Frequency		25.0MHz		HPNA 2.0 can vary this.
	MII_TXCLK Period		40.0ns		
	MII_TXCLK High Time	14.0ns		26.0ns	65/35 Duty Cycle
	MII_TXCLK Low Time	14.0ns		26.0ns	65/35 Duty Cycle
	MII_TXCLK Rise Time	1ns		4ns	
	MII_TXCLK Fall Time	1ns		4ns	
MII Receive Clock					
	MII_RXCLK Frequency		25.0MHz		
	MII_RXCLK Period		40.0ns		
	MII_RXCLK High Time	14.0ns		26.0ns	
	MII_RXCLK Low Time	14.0ns		26.0ns	
	MII_RXCLK Rise Time	1ns		4ns	
	MII_RXCLK Fall Time	1ns		4ns	
MII MDC Clock					

	MII_MDC Frequency	0Hz	2.08MHz	2.5MHz	33MHz/16
	MII_MDC Period	400ns			
	MII_MDC High Time	160ns			
	MII_MDC Low Time	160ns			
	MII_MDC Rise Time	1ns		4ns	
	MII_MDC Fall Time	1ns		4ns	
SMBus Clock					
	SMB_CLK Frequency	0Hz		100KHz	See SMBus Spec.
	SMB_CLK Period	10us			See SMBus Spec.
	SMB_CLK High Time	4.0us		50us	See SMBus Spec.
	SMB_CLK Low Time	4.7us		25ms	See SMBus Spec.
	SMB_CLK Rise Time	1ns		1000ns	See SMBus Spec.
	SMB_CLK Fall Time	1ns		300ns	See SMBus Spec.



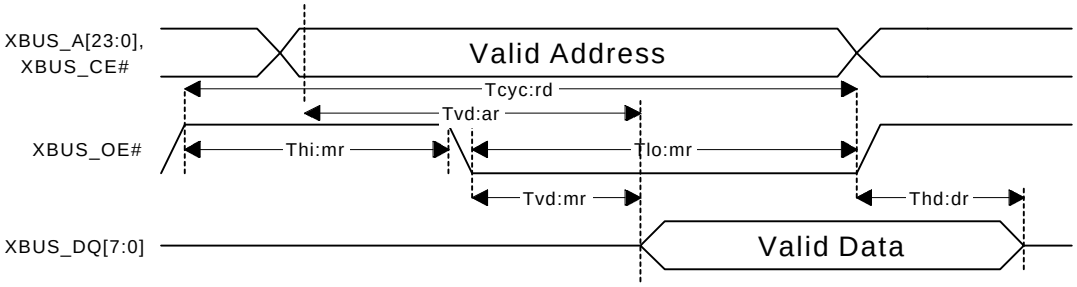
9.4.2 A.C. Interface Characteristics

9.4.2.1 ROM Bus Interface

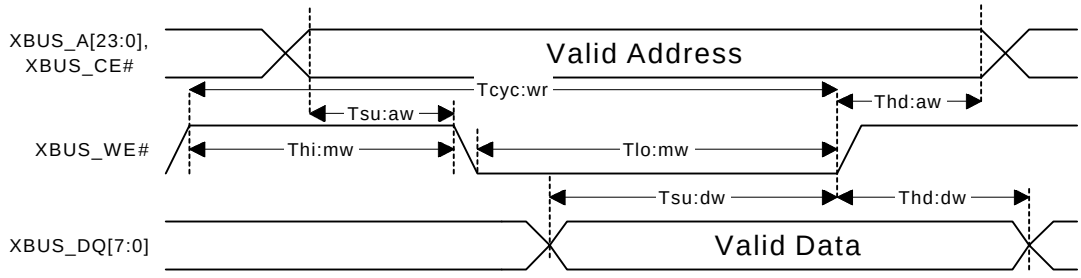
NOTE: The ROM bus has two speeds: 240ns cycle time and 150ns cycle time.

Symbol	Characteristic	High Speed		Low Speed		Comments
		Min	Max	Min	Max	
Tcyc:rd	Read cycle time		150ns		240ns	
Tvd:ar	XBUS_DQ valid delay from XBUS_A, XBUS_CE#		90ns		150ns	
Tvd:mr	XBUS_DQ valid delay from XBUS_OE#		60ns		90ns	
Thd:dr	XBUS_DQ hold from XBUS_OE#, XBUS_CE#, XBUS_A	0ns		0ns		
Tlo:mr	XBUS_OE# active	90ns		150ns		
Thi:mr	XBUS_OE# inactive	60ns		90ns		
Tcyc:wr	Write cycle time		180ns		240ns	
Tsu:aw	XBUS_A setup to XBUS_WE#	60ns		90ns		
Tsu:dw	XBUS_DQ setup to XBUS_WE #	60ns		90ns		
Thd:aw	XBUS_A hold from XBUS_WE #	30ns		30ns		
Thd:dw	XBUS_DQ hold from XBUS_WE #	30ns		30ns		
Tlo:mw	XBUS_WE # active	90ns		120ns		
Thi:mw	XBUS_WE # inactive	90ns		120ns		

ROM Bus Memory Read



ROM Bus Memory Write



9.4.2.2 SMBus Interface

Symbol	Characteristic	Min	Max	Comments
Tlo	Clock low period	4.7us		
Thi	Clock high period	4.0us	50us	See Note 4
Tbuf	Bus Idle Time between Stop and Start Conditions	4.7us		
Thd:sta	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0us		
Tsu:sta	Repeated Start Condition setup time.	4.7us		
Tsu:sto	Stop Condition setup time.	4.0us		
Thd:dat	Data hold time.	300ns		
Tsu:dat	Data setup time	250ns		
Ttimeout	Clock low time-out	25ms	35ms	Note 1
Tlow:sext	Cumulative clock low extend time (slave device)		25ms	Note 2
Tlow:mext	Cumulative clock low extend time (master device)		10ms	Note 3

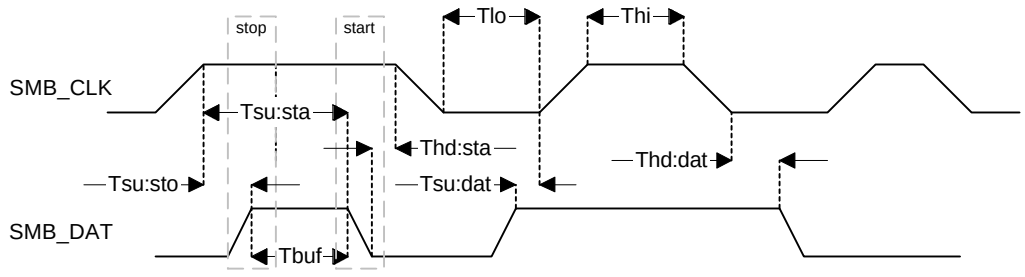
Note 1: Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of Ttimeout-Min. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than Ttimeout-Max. This parameter sets a common point at which a master or slave is allowed to conclude that a defective device is holding the clock low indefinitely.

Note 2: Tlow:sext is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP. It is possible that, another slave device or the master will also extend the clock causing the combined clock low extend time to be greater than Tlow:sext. Therefore, this parameter is measured with the slave device as the sole target of a full-speed master.

Note 3: Tlow:mext is the cumulative time a master device is allowed to extend its clock cycles within *each byte* of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a slave device or another master will also extend the clock causing the combined clock low time to be greater than Tlow:mext on a given byte. Therefore, this parameter is measured with a full speed slave

Note 4: Thigh:max provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock has been high for greater than Thigh:max.

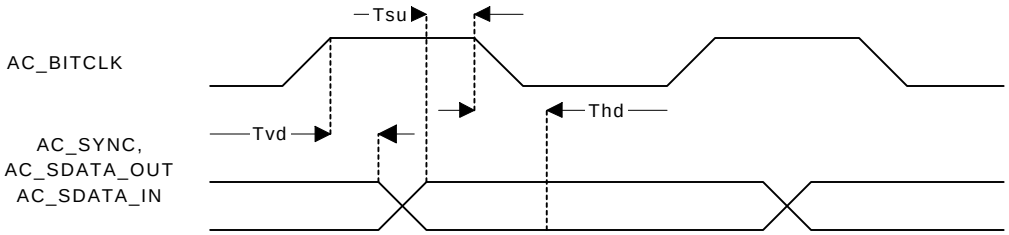
SMBus Timing



9.4.2.3 AC'97 Interface

Symbol	Characteristic	Min	Max	Comments
Tvd	Output Valid Delay from rising edge of AC_BITCLK		15ns	
Tsu	Input Setup to falling edge of AC_BITCLK	10ns		
Thd	Input Hold from falling edge of AC_BITCLK	10ns		

AC'97 Timing



9.4.2.4 USB Interface

Symbol	Characteristic	Min	Max	Comments
	12MHz USB Data Frequency	11.99 Mb/s	12.01 Mb/s	
	1.5MHz USB Data Frequency	1.48 Mb/s	1.52 Mb/s	
Tfl:12	12MHz Data Transition fall time	4ns	20ns	
Trs:12	12MHz Data Transition rise time	4ns	20ns	
Tfl:1.5	1.5MHz Data Transition fall time	75ns	300ns	
Trs:1.5	1.5Mhz Data Transition rise time	75ns	300ns	
Tsk:dr	Source differential skew		5ns	
Tsk:rc	Receiver differential skew		10ns	
	Driver jitter		3ns	
	Receiver jitter		25ns	
	Single-ended driver skew		10ns	

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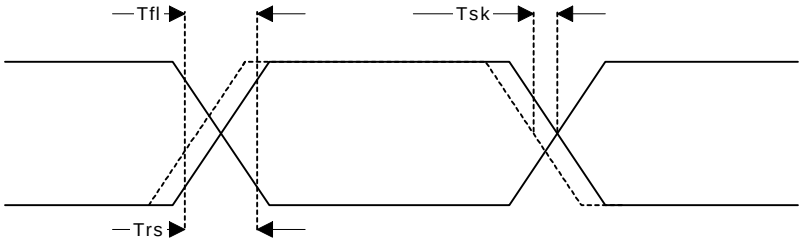
USB Timing

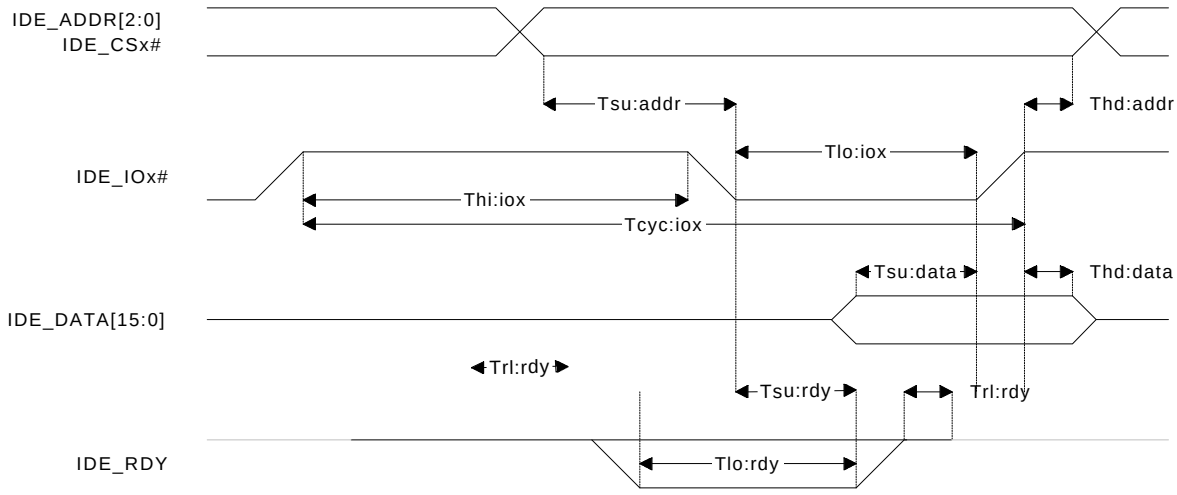


9.4.2.5 IDE Interface

9.4.2.5.1 PIO

Symbol	Characteristic	(ns)	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
Tcyc:iox	Cycle time (IDE_IOx# to IDE_IOx#)	min	600	383	330	180	120
Tsu:addr	IDE_ADDR setup to IDE_IOx#	min	70	50	30	30	25
Thi:iox	IDE_IOx# recovery time	min	-	-	-	70	25
Tsu:data	IDE_DATA write setup to IDE_IOW#	min	60	45	30	30	20
Thd:data	IDE_DATA write hold from IDE_IOW#	min	30	20	15	10	10
Tsu:data	IDE_DATA read setup to IDE_IOR#	min	50	35	20	20	20
Thd:data	IDE_DATA read hold from IDE_IOR#	min	5	5	5	5	5
Thd:addr	IDE_ADDR hold from IDE_IOx#	min	20	15	10	10	10
Tsu:rdy	IDE_RDY setup to IDE_IOx#	min	35	35	35	35	35
Tlo:rdy	IDE_RDY pulse width	max	1250	1250	1250	1250	1250
Trl:rdy	IDE_RDY assertion release	max	5	5	5	5	5
Tlo:iox	IDE_IOx# pulse width 8-bit (register)	min	290	290	290	80	70
Tlo:iox	IDE_IOx# pulse width 16-bit (data)	min	165	125	100	80	70

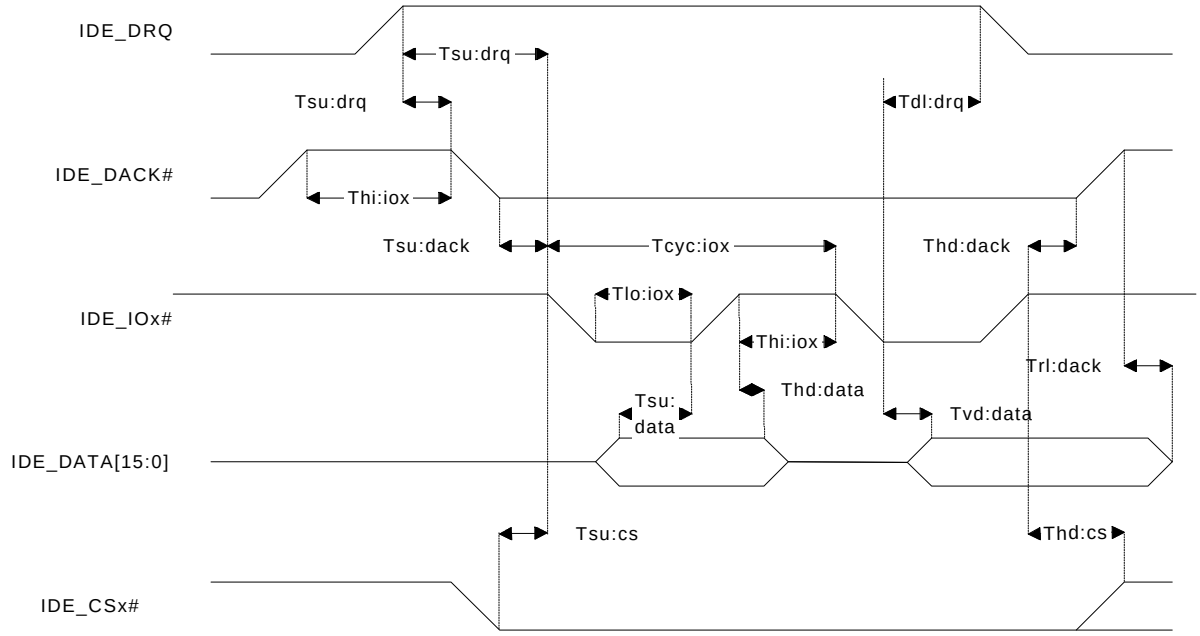
IDE PIO Timing



9.4.2.5.2 Multiword DMA

Symbol	Characteristic	(ns)	Mode 0	Mode 1	Mode 2
Tcyc:iox	Cycle time (IDE_IOx# to IDE_IOx#)	min	480	250	120
Tlo:iox	IDE_IOx# pulse width	min	215	80	70
Tvd:data	IDE_IOR# data access	max	150	60	50
Thd:data	IDE_IOR# data hold	min	5	5	5
Tsu:data	IDE_IOx# data setup	min	100	30	20
Thd:data	IDE_IOW# data hold	min	20	15	10
Tsu:dack	IDE_DACK# to IDE_IOx# setup	min	0	0	0
Thd:dack	IDE_IOx# to IDE_DACK# hold	min	20	5	5
Tlo:iox	IDE_IOR# negative pulse width	min	50	50	25
Tlo:iox	IDE_IOW# negative pulse width	min	215	50	25
Tdl:drq	IDE_IOR# to IDE_DRQ delay	max	120	40	35
Tdl:drq	IDE_IOW# to IDE_DRQ delay	max	40	40	35
Tsu:cs	IDE_CSx# valid to IDE_IOx#	min	50	30	25
Thd:cs	IDE_CSx# hold	min	15	10	10
Trl:dack	IDE_DACK# to read data released	max	20	25	25
Tsu:drq	IDE_DRQ setup		undefined		

DMA IDE Timing



9.4.2.5.3 Ultra DMA

Symbol	Characteristic	(ns)	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
	Typical sustained average two cycle time	min	240	160	120	90	60	-
	Cycle time allowing for asymmetry and clock variations	min	112	73	54	39	25	
	Two cycle time allowing for clock variations	min	230	154	115	86	57	
	Data setup time at recipient	min	15	10	7	7	5	
	Data hold time at recipient	min	5	5	5	5	5	
	Data valid setup time at sender	min	70	48	30	20	6	
	Data valid hold time at sender	min	6	6	6	6	6	
	First STROBE time	min	0	0	0	0	0	
	First STROBE time	max	230	200	170	130	120	
	Limited interlock time	min	0	0	0	0	0	
	Limited interlock time	max	150	150	150	100	100	
	Interlock time with minimum	min	20	20	20	20	20	
	Unlimited interlock time	min	0	0	0	0	0	
	Maximum time allowed from output drivers to release	max	10	10	10	10	10	
	Minimum delay time required for output driver to assert or negate	min	20	20	20	20	20	
	Minimum delay time required for output driver to assert or negate	min	0	0	0	0	0	
	Envelope time	min	20	20	20	20	20	
	Envelope time	max	70	70	70	55	55	
	STROBE to DMARDY# time	max	50	30	20	na	na	
	Ready to final Strobe time	max	75	70	60	60	60	
	Minimum time to assert STOP or negate IDE_DACK#	min	160	125	100	100	100	
	Maximum time before releasing IDE_RDY#	max	20	20	20	20	20	
	Maximum time before releasing STROBE	min	0	0	0	0	0	
	Setup and hold times for IDE_DACK#	min	20	20	20	20	20	
	Time from STROBE edge to negation of IDE_REQ# or assertion of STOP	min	50	50	50	50	50	

10.0 Package

The MCP-1 is available in a 23x23mm 376 PBGA package. The ball array is 5 rows deep (340) with a 6x6 core array of power/ground balls in the center (36). It has a 1mm ball pitch. All package dimensions are given in the Table and shown in the Figures below.

Table 2 376 PBGA Package Dimensions

Ref.	Millimeters		
	Minimum	Typical	Maximum
A	**2.03**	**2.23**	**2.43**
A1	**0.40**	**0.50**	**0.60**
A2	**1.12**	**1.17**	**1.22**
b	**0.50**	**0.60**	**0.70**
C	**0.51**	**0.56**	**0.61**
D	**22.80**	**23.00**	**23.20**
D1	**21.00 BSC**		
D2	**19.30**	**19.50**	**19.70**
D3	**14.70**		
E	**22.80**	**23.00**	**23.20**
E1	**21.00 BSC**		
E2	**19.30**	**19.50**	**19.70**
E3	**14.70**		
e	**1.00 BASIC**		
T	**30 TYP**		

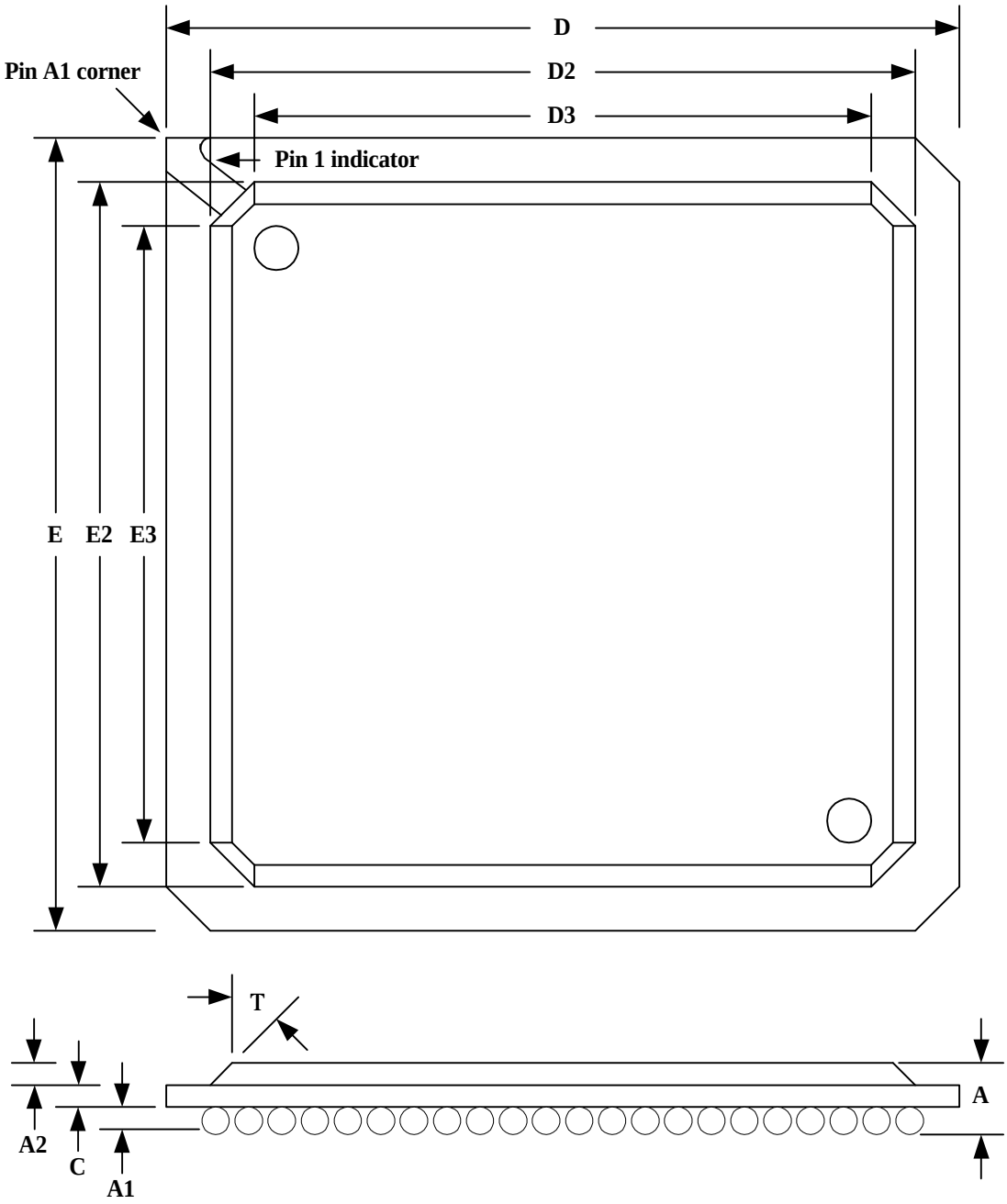


Figure 1 376 PBGA Package Top View

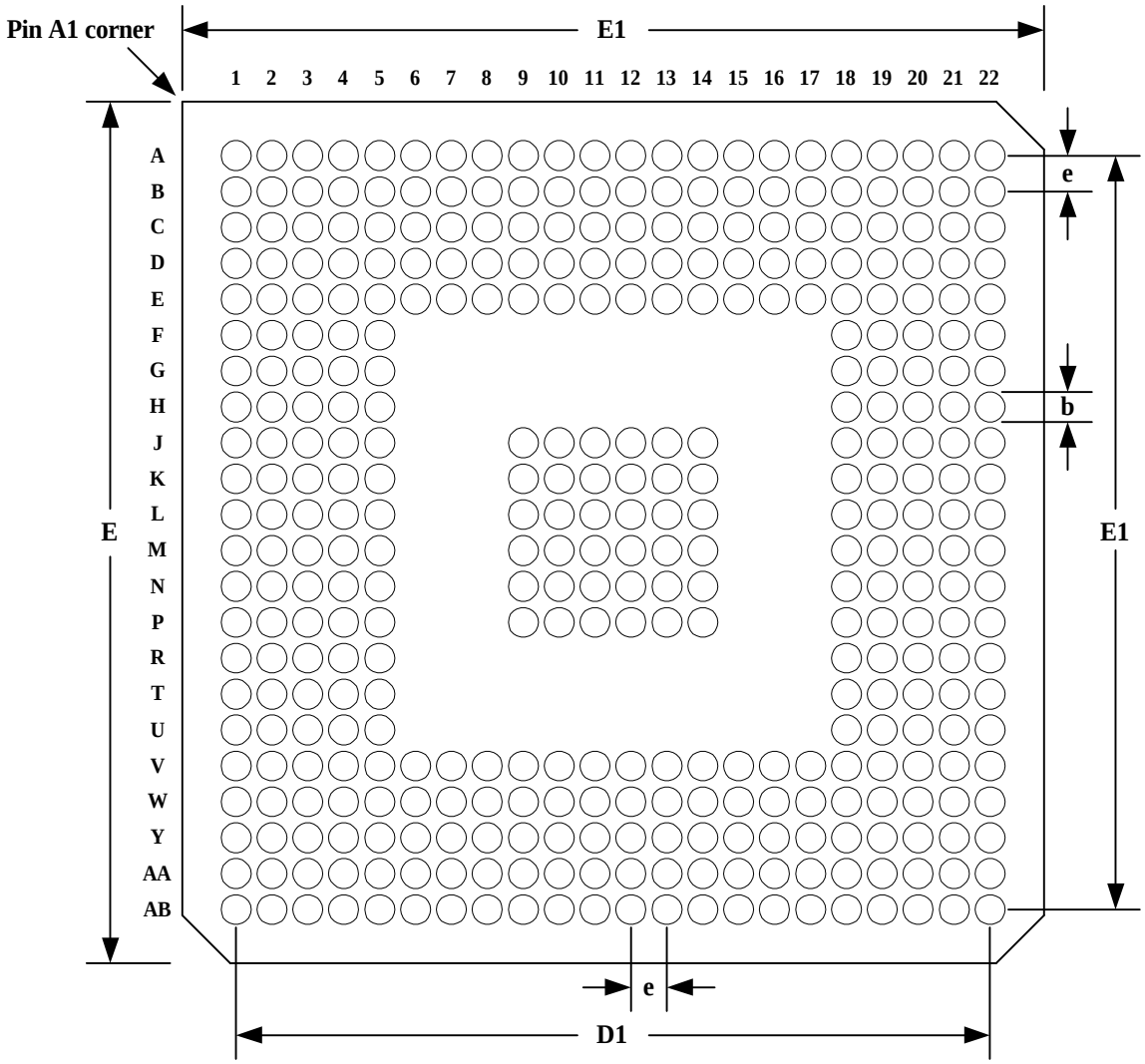


Figure 2 376 PBGA Package Bottom View

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