Hardware Design Specification

Project: Xbox

Author: leodelc, ggibson

Revision: 0.91

Date: 11/2/2000

Proprietary Notice

Published by

X-box Console Group

Microsoft Corporation
One Microsoft Way
Redmond, WA 98052-6399
Telephone (425) 882-8080

Contents

1. OVERVIEW 12

1.1. Xbox Game System Architecture 13

1.2. Xbox Console Architecture 14

1.3. Software Architecture 15

1.4. Front Panel Features 15

1.4.1. Power Switch 15

1.4.2. Game Controller Ports 16

1.4.3. Disk Eject 16

1.4.4. Indicator Lights 16

1.5. Rear Panel Features 16

1.5.1. Power IN 16

1.5.2. Audio Video Interface Port (AVIP) 16

1.5.3. Network Interface 16

1.6. System Durability Requirements 17

1.6.1. Reliability Requirements 17

1.6.2. Environmental Requirements 18

1.6.3. Shipping Requirements 19

2. DESIGN SPECIFICATIONS 20

2.1. Central Processing Unit 20

2.2. System Memory 20

2.3. Boot ROM 21

2.4. Graphics Subsystem 21

2.4.1. North Bridge and GPU (NV2A) 22

2.4.2. TV Encoder 24

2.5. Audio Subsystem 26

2.5.1. Audio Processing Unit 27

2.5.2. Digital Audio Interface Controller 28

2.6. Core Logic (MCPX) 29

2.6.1. Audio Processor and Digital Audio Interface 30

2.6.2. ATA Interface 30
2.6.3. USB Host Controller 30
2.6.4. Ethernet MAC 30
2.6.5. General Purpose IO Pins 31
2.6.6. Internal Boot ROM 31
2.6.7. External ROM Interface 32
2.6.8. LPC Interface 32
2.6.9. LDT Bus 32
2.6.10. Clock Generator 33
2.6.11. Real Time Clock (RTC) 33
2.6.12. CPU Support Logic 34

2.7. System Management Controller 36
2.7.1. Pin Out 37
2.7.2. Power Control 38
2.7.3. Temperature Monitoring 39
2.7.4. Fan Control 39
2.7.5. Front Panel IO 40
2.7.6. AV Mode Detect 42
2.7.7. DVD Tray Control 43

2.8. System Clocking 43
2.8.1. System Clocking Architecture 43
2.8.2. Clock Generator 44
2.8.3. RTC Clock Specifications 47

2.9. Digital Versatile Disk (DVD) Drive 47
2.9.1. Media Compatibility 47
2.9.2. Format Compatibility 48
2.9.3. Spindle Speed Control 48
2.9.4. Performance Specifications 48
2.9.5. Electrical Specifications 51
2.9.6. Functional Requirements 54
2.9.7. Software Requirements 56
2.9.8. Mechanical Specifications 57
2.9.9. Environmental Requirements 57

2.10. Hard Disk Drive (HDD) 57
2.10.1. General Specifications 57

2.10.2. Performance Requirements 58
2.10.3. Electrical Requirements 59
2.10.4. Environment Requirements 59
2.11. Network Interface 59
2.11.1. Ethernet PHY 59
2.11.2. Magnetics Specification 60
2.11.3. Network Connector 61
2.11.4. Interface Circuit 61
2.12. Audio Video Interface Port (AVIP) 62
2.12.1. Mechanical Connector Characteristics 62
2.12.2. DC Power Output 65
2.12.3. Mode Selection Inputs 65
2.12.4. Digital Audio Output 65
2.12.5. Analog Audio Output 66
2.12.6. Video Outputs 68
2.12.7. SCART Status Output 73
2.13. Controller Interface Port 75
2.13.1. Mechanical Specification 75
2.13.2. DC Power Output 76
2.13.3. Digital Communication 78
2.13.4. Video Sync Signal 78
2.14. LPC Header 78
2.14.1. Mechanical Specification 79
2.14.2. Signal List 80
2.15. Power Supply 80
2.15.1. System Power Budget 81
2.15.2. System PSU 81
2.15.3. RTC Power Supply 83
2.15.4. Local Voltage Regulators 84
3. XBOX ACCESSORIES 86
3.1. Game Controller 86
3.2. AV Packs 86
4. SYSTEM INTEGRATION 93

4.1. Motherboard Printed Circuit Board Assembly 94
4.1.1. System Power 94
4.1.2. ATA 95
4.1.3. Controller 1/2 Port 95
4.1.4. Controller 3/4 Port 95
4.1.5. Front Panel 96
4.1.6. DVD Power/Control 96
4.1.7. Fan 97
4.2. System Fan Assembly 97
4.3. Front Panel IO Subassembly 98
4.4. Dual Controller Port Subassembly 99
4.5. System PSU 99
4.5.1. System Power 99
4.5.2. HDD Power Harness 100
4.6. DVD Drive 101
4.6.1. ATA Connector 101
4.6.2. Power/Control Connector 101
4.7. DVD Power/Control Cable Assembly 101
4.8. Hard Disk Drive 102
4.8.1. ATA Connector 102
4.8.2. Power Connector 102
4.9. ATA Cable Assembly 102
APPENDIX A – POWER BUDGET SPREADSHEET 103
APPENDIX B – SYSTEM MEMORY MAP 105
APPENDIX C – SM BUS ADDRESS MAP 106
APPENDIX D – TELEVISION SYSTEMS USED BY COUNTRY 107
APPENDIX E – VIDEO WAVEFORM TIMING 108
APPENDIX F – SAFE ACTION AND SAFE TITLE GUIDELINES 109
APPENDIX G – SYSTEM RESET FLOW CONTROL 110

Revision History

Revision	*Date*	*Description*	*Author/Revised by*
0.1	10/11/1999	Initial draft based on preliminary work of exploratory team, presentations, and meeting notes	leodelc
0.2	10/14/99	Added detail	leodelc, ggibson
0.3	10/25/99	Reviewed at potential supplier	leodelc, ggibson
0.4	10/26/99	Updated during manufacturing review	leodelc
0.5	10/28/99	Minor updates	ggibson
0.51	10/29/99	Removed references to 3rd party component names & features	ggibson
0.61	11/12/99	Revise front and rear panel connection requirements, a/v connector requirements, and audio requirements	leodelc
0.62	11/22/99	Added 1394 & USB to rear panel; updated power supply section	ggibson
0.63	11/24/99	Updated AV Pack descriptions	leodelc
0.64	12/10/99	Added HDD detailed specification. Added system reliability, environmental and shipping specifications	leodelc
0.65	1/12/00	Updated block diagram to reflect recent major product definition decisions. Eliminate 1394, Modem. Integrate NB logic into GPU UMA Eliminate HDTV requirements Added SMBus requirement to core logic.	leodelc
0.66	2/16/00	Incorporate details from motherboard kickoff meeting. Completed preliminary detailed power budget and PSU specification.	leodelc
0.67	2/25/00	Added Modem requirements and improved HDD and DVD drive requirements section	leodelc
0.68	3/2/00	Updated per MRD AV Pack specs complete	leodelc
0.69	3/15/00	Added Video output requirements Updated DVD drive spec detail Eliminated RESET switch	leodelc

Revision	*Date*	*Description*	*Author/Revised by*
0.7	4/14/00	Added core logic descriptions and added detail for DVD, modem, TV encoder, and audio codec	leodelc
0.71	5/1/00	Added detail	leodelc
0.72	5/10/00	Updated DVD specification based on vendor feedback	leodelc
0.73	5/18/00	Updated based on MCPX review and additional feedback	leodelc
		Introduced a new section for system integration and definitions for major system sub assemblies	
		Updated AV Pack configurations	
0.74	5/30/00	Updated system PSU spec	leodelc
		Eliminated VESA AV Pack	
		Added system clocking architecture	
0.75	7/5/00	Eliminated redundant specifications covered in detailed documents (PSU, DVD)	leodelc
		Updated system assembly details	
		Updated AVIP pinout to optimize motherboard layout	
		Updated video filter requirements	
0.9	7/28/00	Updated Modem spec	leodelc
		Updated AV Pack specs	
		Updated ATA cable lengths	
		PIT clock defined @25MHz	
		Added APICLK requirement	
		Incorporated feedback from Intel review	
		Removed rear expansion port	
		HW initialization region in boot ROM increased to 256 bytes	
		Added system RESET, SMBus, Interrupt mapping	
		Swapped DVDEJECT and SMI on SMC pinout.	
0.91	10/19/00	Updated based on input from team review	leodelc

Reference Documents

This document references the following documents:

Microsoft Specifications Documents

System Management Controller Firmware Specification, Revision 0.2, 9/26/2000

DVD-ROM Drive Specification, Revision 0.85, 6/19/2000

Power Supply Design Specification, Revision 0.92, 8/3/2000

Xbox 3rd Party Game Controller Specification, Doc No. QQ101Revision 0.92, August 23, 2000

Component Data Sheets

Desktop Pentium(R) III Processor in BGA2 Package Electrical, Mechanical, and Thermal Specification. Intel Reference Number FM-1923

NV2A (Xbox Graphics Processing Unit) Design Specification, Revision 0.5, September 11, 2000

Flicker-Free Video Encoder with Ultrascale Technology, Conexant Document Number 100381A, February 2000

MCP-1 Media Communication Processor (South Bridge), Version 0.15, August 2000

LXT972A 3.3V Dual-Speed Fast Ethernet Transceiver, Revision 1.1, Level One Document Number IS972DS-R1.1-0200, February 2000

AC-Link Interface Audio DAC, WM9709 Advance Information, Rev 1.0, June 2000

Quad USB High-Side Power Switch With Fault Detection, IMP2524/7, IMP Publication #5005 Rev A, 5/17/00

Low Resistance USB High-Side Power Switch, IMP Publication #5001 Rev A, 10/27/99

Lithium Batteries Handbook, Panasonic, August 1998

8-Bit CMOS Microcontrollers with A/D Converter, PIC16C63A/65B/73B/74B, Microchip DS30605B

Molex Connector,

U Series 5 Family Product Manual, Seagate Publication Number: 20400172-001, Rev. B, August 2000

Western Digital EIDE Hard Drive, WD Protégé Technical Reference Manual, Western Digital Document Number 2679-001008-000, 9/7/00

Dual PUSB Cable Harness, Foxlink P/N PU23310-C, Rev 0.1

Mechanical Package Specification Candyland Control PCB,

Fiber Optic Transmitter Module, TOTX178A, Toshiba, 2000-02-18

Industry Standards Documents

Standard Definition TV Analog Component Interface, EIA-770.2-A, December 1999

High Definition TV Analog Component Video Interface, EIA-770.3, September 1998

120mm DVD Read-Only Disk, Standard ECMA-267, 2nd Edition, December 1999

80mm DVD Read-Only Disk, Standard ECMA-268, 2nd Edition, December 1999.

AT Attachment with Packet Interface Extension - (ATA/ATAPI-4), ANSI NCITS 317-1998

Suite of 3.5" Form Factor Specifications, ANSI SFF-8300, Rev 1.1, June 5, 1995

Specification for ATA 40-pin Connector, ANSI SFF-8059, Rev 2.5, July 31, 1998

Digital audio interface – Part 1 General, IEC 60958-1,

Digital audio interface – Part 3 Consumer Applications, IEC 60958-3,

Audio, video and audiovisual systems - Interconnections and matching values - Preferred matching values of analogue signals, IEC-61938,

Universal Serial Bus Specification, Version 1.1

IEC-60320, Power inlet defintion

IEEE 802.3, Ethernet spec

Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29, 1997

Installable LPC Debug Module Design Guide, Revision 1.0, Intel,

IEC-60320

IEEE 802.3u

ANSI SFF 8059

This reference list in incomplete

Approvals

Approved by:		Date:	
	Todd Holmdahl, HW Development Manager		
Approved by:		Date:	
	Leonardo Del Castillo, Electrical Engineering		
Approved by:		Date:	
	Greg Gibson, Electrical Engineering		
Approved by:		Date:	
	Rob Walker, Electrical Engineering		
Approved by:		Date:	
	Woody Beverly, Firmware Engineering		
Approved by:		Date:	
	Jeff Reents, Mechanical Engineering		
Approved by:		Date:	
	Dick Liu, Mechanical Engineering		
Approved by:		Date:	
	Jon Wilcox, HW Test Lead		
Approved by:		Date:	
	Jim Stewart, Industrial Design		
Approved by:		Date:	
	Tom Brooks, Usability		
Approved by:		Date:	
	Jon Thomason, Software Development Manager		
Approved by:		Date:	
Approved by:		Date:	
Approved by:		Date:	

1. Overview

The Xbox is a variation of the legacy-free PC architecture designed to target the game console and living room entertainment space. The Xbox product definition targets four key aspects, including minimal retail price, excellent graphics and sound performance, enhanced television viewing, and Internet capability.

This document specifies the hardware design of the Xbox gaming console, including specification of the following system-critical design aspects:

- Central Processing Unit (CPU)
- Main memory cache capacity and performance
- Main memory capacity and bandwidth
- 3-D Accelerated Graphics Processor architecture, performance and memory capacity
- 3-D Accelerated Audio Processor
- Audio and Video Outputs
- Universal Serial Bus implementation
- Digital Versatile Disk specification
- Boot-ROM implementation
- Hard Disk Drive specification
- Core logic implementation

The architecture of the Xbox is based on leading edge PC technology. The architecture and performance of the Xbox shall remain constant through the life span of the product, which is estimated at approximately 4 years. Over this span of time, PC technology will continue to advance, while average PC prices fall at a fairly low rate. The Xbox, however, shall maintain consistent performance year over year, while decreasing the cost of manufacture and the retail price of the product.

The long-term requirements of the design are:

- Fast time to market of initial design
- Rock-solid reliability
- Best-in-class performance compared to current PC designs
- Significantly better performance relative to contemporary game consoles
- Path to achieve cost reduction of 30% annually
- Uniform performance over time, independent of implementation

1.1. Xbox Game System Architecture

The Xbox game system consists of the Xbox console, one or more game controllers, an AV Pack, a television monitor, and an audio reproduction system. Refer to the diagram below for the following description of the game system, the components involved, and their interconnection.

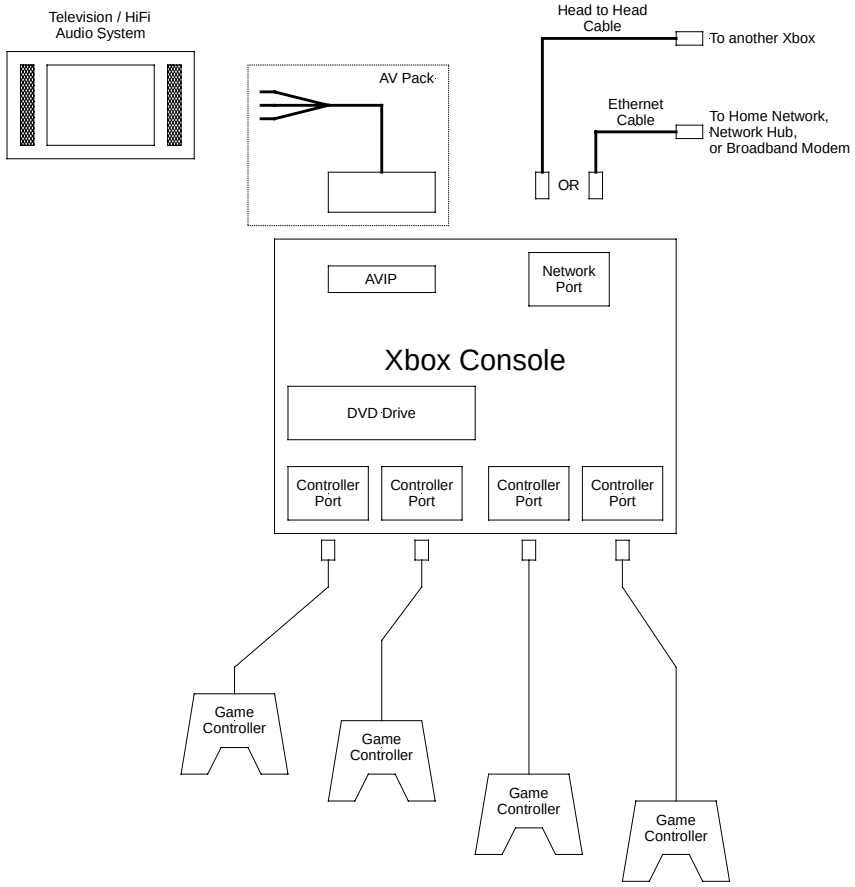


Figure 1. Xbox Game System

The Xbox game console has three interface ports; controller interface ports, the Audio Video Interface Port (AVIP), and the network port. The controller ports, located on the front of the console provide a means of connecting game controllers to the console. Game controllers are the primary user input devices for the console. The AVIP is a multi-pin connector that carries all the signals required to connect the Xbox console to a television and audio system. The Xbox supports many type of interconnection methods. An AV Pack is an accessory device that adapts the AVIP to the particular needs of the user's audio visual system. There are AV Packs that provide composite video and line level audio signals, RF modulated signal, and high-quality component video signals.

The network interface port provides a means of networking several Xbox consoles together for head to head or group game play. Networking may be peer-to-peer, local area network, or broadband via the Internet.

1.2. Xbox Console Architecture

The figure below shows the system-level block diagram of the Xbox console.

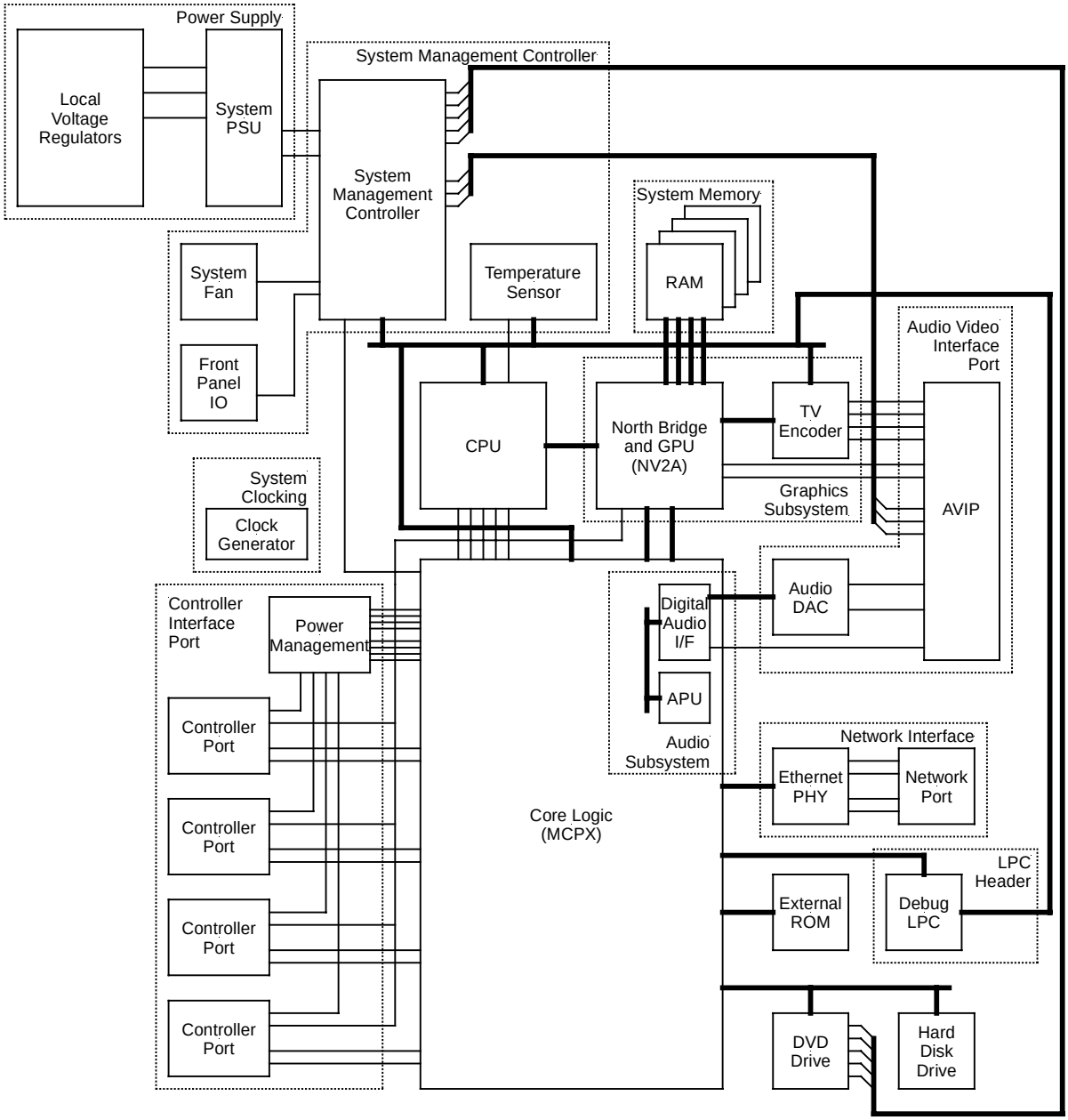


Figure 2. Xbox System Block Diagram

The remainder of this section describes the features of the Xbox design. Subsequent sections shall describe the detailed design and implementation guidelines and performance specifications required to implement the described feature set.

1.3. Software Architecture

This document does not presume to cover the detailed software architecture of the Xbox, but the following sections provide a high-level overview of the architecture of the OS, and how it is related to the hardware design of Xbox for the first and following years.

The Xbox Operation System is divided into two pieces, the XROM and the Xbox Title Library (XTL). The XROM is the kernel of the XOS operating system. It provides the hardware initialization code, XOS kernel, decryption and code signature verification, application loading, and the drivers for some of the hardware features. The XTL is provided to the application developer as a linkable library, becoming part of the executable code loaded from the DVD media. The XROM is specific to a particular console design, whereas the XTL is generic and must be able to work with any iteration of the Xbox hardware design.

An Xbox application primarily controls and configures the Xbox hardware by calling the XOS API, however, an application may also access some parts of the Xbox hardware directly, in an effort to provide the most efficient performance. For the performance-critical features of the Xbox, the hardware implementation will remain exactly the same, and so direct access to these hardware features will be the same throughout the product life of the Xbox. In general, any hardware feature normally handled by the XTL may also be accessed directly by the application.

Some aspects of the Xbox hardware design, however, have no impact on application performance, and may undergo changes from year to year as the Xbox design is cost optimized. The code to configure, control, and communicate with these features is implemented in the XROM. An application must never directly access these hardware features.

The components that must never be accessed directly by the application are listed below:

- System Management Controller
- Ethernet PHY Transceiver
- TV Encoder
- DVD drive
- Hard Disk Drive
- Second USB Host Controller
- Real Time Clock
- GPIO pins of the MCPX
- Ethernet MAC

1.4. Front Panel Features

This section briefly describes the features of the Xbox console at the system level. A detailed description of the functionality, implementation, and specifications for each feature can be found in the later sections of this document.

1.4.1. Power Switch

The power switch is a momentary type push switch, monitored by the System Management Controller (SMC), which in turn monitors the system power up and power down cycle. The design implements soft power up and power down, allowing the system to perform cleanup operations prior to shutdown. At the same time, the SMC guarantees the system will shut down reliably in the case of a system crash.

The Xbox does not implement any meta-power states. The console itself is either “on” or “off”, although the SMC is always on as long as mains power is applied.

1.4.2. Game Controller Ports

Four front-mounted game controller ports are required. Electrically, each port appears as a full-speed upstream USB port, but mechanically, the connector is proprietary. The proprietary connector is designed to meet the Xbox product requirements for pull force and cycle life.

1.4.3. Disk Eject

The disk eject button is also monitored by the SMC. This allows the disk eject function to be operated even if the power is “off”, so long as mains power is applied.

1.4.4. Indicator Lights

The EJECT switch is surrounded by a light pipe illuminated by a pair of red and green LEDs. The LEDs are controlled by the SMC based on the SMC state machine and software settings requested by the CPU. The behavior of these LEDs is described in detail in the SMC section.

1.5. Rear Panel Features

1.5.1. Power IN

The power input shall be AC line power, via a removable 2-pin line cord conforming to IEC-60320 2.5A Plug Connector for Class II Equipment. The input voltage range shall be constrained to “low range” (approximately 110V) or “high range” (approximately 240V) depending on the regional market in which the console is sold.

1.5.2. Audio Video Interface Port (AVIP)

This multi-pin port consists of all electrical input and output ports supported by the graphics processor and audio codec. The AVIP includes video output signals, audio output signals, and selector inputs used to identify the type of adapter connected to the AVIP port.

By setting the logic states of the AVIP inputs, the adapter may select CVBS+Y/C (NTSC, PAL, or SECAM), CVBS + RGB (PAL SCART) or YPrPb HDTV outputs. The AVIP has two audio interface ports; line-level stereo audio (left and right channels) is output directly, and a logic-level SPDIF output is provided for interface to an external coaxial or fiber optic driver.

1.5.3. Network Interface

The network interface is implemented as a 10/100-Base T (RJ-45) Ethernet port. This port provides access to broadband Internet connections such as cable modems, DSL modems, home networks, and peer-to-peer networking. The PHY layer and MAC shall support 10 and 100 Mbit/s operation (IEEE 802.3u).

1.6. System Durability Requirements

This section describes the system environmental and reliability requirements. This section is provided only for reference, the actual requirements of the electrical design will be affected by the mechanical enclosure and thermal management system.

1.6.1. Reliability Requirements

	Spec Requirement	**Comments**
Mean Product Life	9000 hrs @ 25C 2000 hrs @ 45C	Product warranty will be 90 days Mean life represents operational hours at indicated ambient temperatures
Total DPM	10,000	Total yield, including infant mortality
Factory DPM	5000	
30-day Infant Mortality DPM	5000	
Mean Time To Failure	250k hours @ 25C	This figure represents the steady-state failure rate of units in the field, excluding infant failures and end of life failures. The failure rate for 5M units used 4hrs/day ≈ 30k units/year
Service Life	8000 hrs @ 25C 2000 hrs @ 45C	This corresponds to 4-5 hours per day for 5 years.
Connector reliability	2000 cycles	All user-accessible connectors
DVD loader reliability	10,000 load/unload cycles	This may need to be increased based on typical usage scenario.
DVD Eject Button	20,000 cycles	This may be reduced as this level of reliability may exceed the typical usage scenario.
Power cycling and switch reliability	20,000 cycles	This may be reduced as this level of reliability may exceed the typical usage scenario.
Power switch bounce	10ms max.	

1.6.2. Environmental Requirements

	Spec Requirement	Comments
Operating Temperature	5 to 45C	External ambient air temperature. Assume box is placed on a hard surface that is at thermal equilibrium with the ambient air.
Operating Humidity	5 to 85%RH	Non-condensing
Operating Altitude	0 to +2,000 m	Relative to Mean Sea Level
Maximum operating tilt	10°	The unit may be tilted from the horizontal plane up to this angle in any direction.
Maximum power dissipation	200W	Input power to the unit.
Harmonic Current Emissions	Per IEC-61000-3-2 as required by locale	European and Japanese versions of the product are subject to this standard.
Max external case temperature	50C (buttons) 60C (case)	Measured at any point on the external surface, at an external ambient temperature of 25°C. Installed per IEC-60065.
System Acoustic Noise (Nominal conditions)	< 32dB measured @ 1m (< 28dB Goal)	Measured in anechoic chamber with background noise level at least 10dBA below the expected measured level. This measurement made at standard operating conditions of T_A=25C, with the DVD drive reading sequential tracks on the disk, and the HDD spinning idle.
Thermal Shock	-40 to 60°C, 40C/min ramp, 100 cycles with power applied	No functional failures allowed. The thermal gradient is maintained without condensation.
Unit Drop	3 random drops from 75 cm on to 6mm carpet over ¾" plywood @ 20-25C	Failure is considered functional damage that is not obviously repairable by the end user. There are no cosmetic requirements after drop testing.
Chemical Resistance	Resistant to short-term exposure to common household cleaning agents, including isopropyl alcohol, coffee and cola. Resistance to anything commonly found on the human hand, or used to clean consumer electronics	Acceptance is determined by functional performance only (no cosmetic requirements). Chemicals shall be applied only to outside surfaces for a period of less than one minute. This specification applies to the external cosmetic surfaces, and does not imply intrusion of chemicals into the interior of the chassis.
UV Stability	Per ASTM D4674-89	No material degradation allowed. Color changes are acceptable (no requirement). It is desired to restrict color changes to a delta-E less than 1.0.

A "Functional Failure" is considered to be any permanent component failure that results in the unit becoming unserviceable by the end user. Transient failures during operation, i.e. unit locks up, crashes, or resets, is not considered a functional failure if the user can clear the condition by cycling the power ON switch.

1.6.3. Shipping Requirements

	Spec Requirement	Comments
Package Drop	10 drops, 92cm onto asphalt tile over concrete	No functional or cosmetic failures allowed.
Package Shock (non-operational)	60 minutes per ASTM D999	No functional or cosmetic failures allowed.
Package Vibration	Random, see H00232	No functional or cosmetic failures allowed.
Storage Temperature	-40 to 60°C	No functional or cosmetic failures allowed.
Storage Humidity Up to 50°C Ambient Above 50°C Ambient	 5 to 90%RH 5 to 70%RH	Non-condensing in all cases. No functional or cosmetic failures allowed.
Storage Altitude	-300 to +12,000m	Relative to Mean Sea Level

2. Design Specifications

2.1. Central Processing Unit

The Xbox CPU is an Intel PIII variant based on the Coppermine CPU. The CPU features:

MMX and SSE instruction set enhancements

733MHz internal clock rate

133MHz Front-Side Bus

32k L1 Cache

128k Full-speed L2 Cache integrated on-die

BGA-2 package

Manufactured in a 0.18µ process in the first year of production, with possible die shrink in following years.

JTAG

For a detailed data sheet, refer to the *Desktop Pentium(R) III Processor in BGA2 Package Electrical, Mechanical, and Thermal Specification* published by Intel. The top-level power requirements are listed below:

Parameter	Min	Typical	Max	Unit
Core Power Supply VCC_{CORE} ICC_{CORE}		1.75	 14.6	 V A
AGTL Bus Termination Voltage Supply V_{TT} I_{TT}	1.365	1.50	1.635 2.7	 V A
Total Power Consumption			26	W

Figure 3. CPU Electrical Characteristics

2.2. System Memory

Xbox uses a unified memory architecture (UMA) to consolidate the system RAM and graphics RAM in to a single memory pool. An advanced memory controller and bus arbitration unit bridges the CPU system bus and the GPU system bus and provides high-speed access to the unified memory pool.

The system will use DDR SDRAM (Double Data Rate Synchronous Dynamic Random Access Memory) memory. DDR SDRAM transfers data words at a sustained 400MHz, using both edges of the 200MHz memory clock.

The size of the unified memory pool is 64MB. The memory space is divided into four fully independent memory channels, each 32-bits wide and capable of four open pages of memory.

The RAM IC's will be soldered directly on to the motherboard to eliminate the need for sockets and DIMM modules. The board layout will incorporate eight 2Mx32 ICs, two on each of the four data channels. The two IC's on each bus will be located opposite each other on top and bottom side of the board, with connections made between closest pins. Since address and data pins will be crossed in this configuration, the memory controller will compensate by multiplexing the pin assignments depending on whether it is accessing the top-side or bottom-side IC. Future redesigns

of the Xbox motherboard may migrate to 4Meg x 32 ICs, but the total number of open pages will remain the same.

The DDR memory bus has the following characteristics:

Parameter	Specification
Data transfer rate	1.6GB/s per channel, 6.4 GB/s combined
Bus Speed	200 MHz DDR
Bus Width (Data)	4x32 bits (128 bits total)
Voltage	approximately 2.5V
Parity	None

Note: Detail of the system memory components and specification is pending component qualification and vendor selection.

2.3. Boot ROM

The Xbox does not have a traditional BIOS such as found in a traditional PC. Instead, the Xbox boots directly from a Flash-RAM or ROM containing hardware initialization code and the Xbox Operating System (XOS). Early production units will implement the Boot ROM as Flash Memory, but will later migrate to a ROM-based component to minimize cost. The Boot ROM shall not be field-upgradeable or modifiable by the user without disassembly and electrical access to the motherboard.

The XOS shall occupy no more than 1M bytes of ROM. The Boot ROM is interfaced through the core logic. The upper 512 bytes of the 1M space is mapped to ROM internal to the MCPX. The lower 256 bytes of the Boot ROM are reserved for hardware initialization values for the MCPX and NV2A core logic chips. These locations will be read directly by the core logic chips prior to CPU reset.

2.4. Graphics Subsystem

The graphics subsystem consists of a high-performance memory controller integrated with an advanced graphics processor and a digital video interface to the television encoder. The television encoder includes digital scaling and encoder logic as well as the digital to analog converters for producing NTSC/PAL/SECAM television signals and component YPrPb HDTV signals.

The north bridge functionality is integrated with the graphics processor to implement a Unified Memory Architecture (UMA). The North Bridge consists of a memory controller, a P6 front-side bus interface, an LDT interface, and an arbitration unit to route transactions across the CPU, GPU, LDT, and memory busses. The bus connecting the arbitration unit and the GPU memory bus is internal to the IC. The LDT interface is used to bridge to the companion core logic chip containing the lower-bandwidth logic functions such as ATA, USB, XROM, and the APU. These functions are described in more detail in a subsequent section.

The performance level of the graphics processor is representative of DirectX 8 class PC products. The overall system performance is not only a function of the graphics processor, but also of the busses that interconnect the graphics subsystem and the CPU. The detailed performance criterion for the graphics subsystem components is described in the following sections.

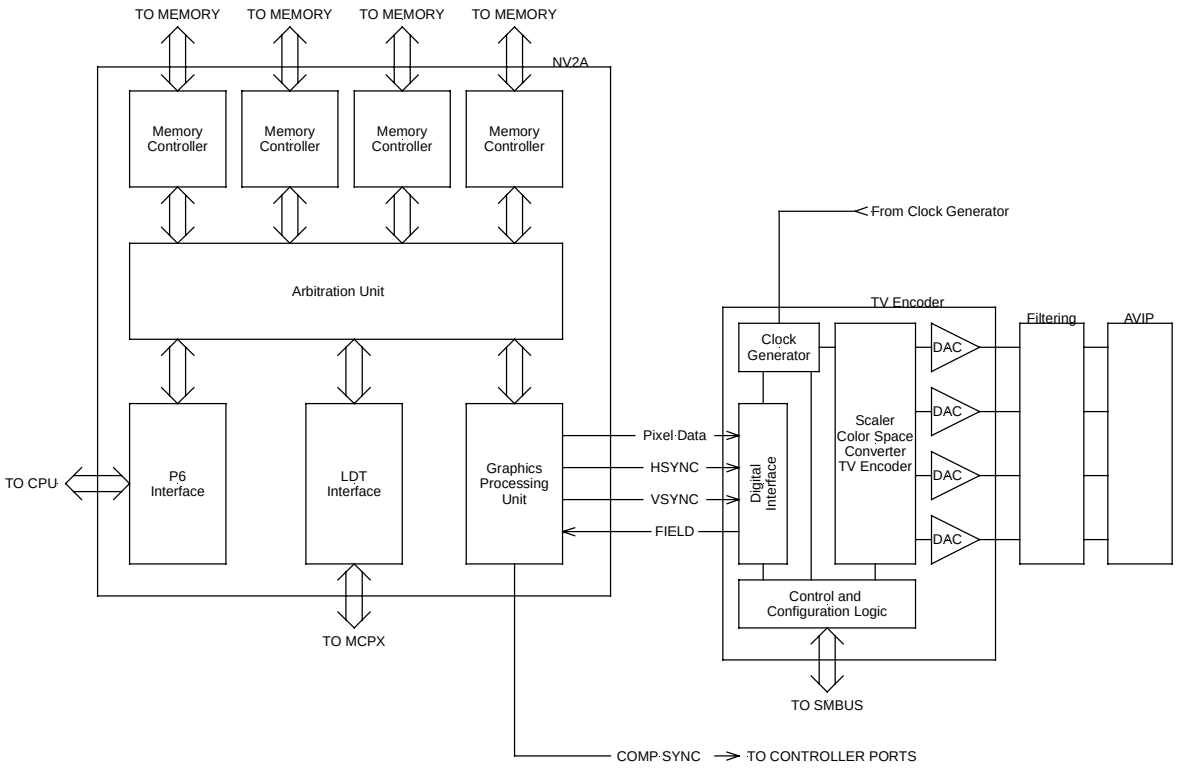


Figure 4. Graphics Subsystem Block Diagram

2.4.1. North Bridge and GPU (NV2A)

The NV2A is an integrated North Bridge memory controller and Graphics Processor Unit. The NV2A contains four independent memory controllers for the unified system memory, a P6 front-side bus interface to the CPU, an LDT bus interface to the core logic, a GPU, and an arbitration unit to manage memory and inter-bus transactions.

Refer to the *NV2A Design Specification* for detailed electrical, thermal, and mechanical characteristics. The table below summarizes the system-level characteristics of the NV2A.

Parameter	Min	Typical	Max	Unit
Core and LDT Power Supply V1P5 I_{V1P5} Power Consumption	1.45	1.50	1.55 7 8.4	 V A W
LVTTL Interface Supply V3P3 I_{V3P3} Power Consumption	3.0	3.3	3.6 TBD TBD	 V A W
CPU AGTL+ Termination Supply VAGTL I_{VAGTL} Power Consumption	1.385	1.5	1.615 TBD TBD	 V A W
Memory Interface Power Supply V2P5 I_{V2P5} Power Consumption	2.3	2.5	2.7 1.5 4	 V A W
Total Power Consumption			15	W

Figure 5. GPU Electrical Characteristics

Parameter	Specification
Package	PBGA, 680 balls max at 1mm pitch, 35x35mm
Ball-Out Configuration	5 rows of signal balls (580 balls), 10x10 central thermal GND array
Construction	Encapsulated die, Chip up with bond wire substrate
Substrate	4-layer
Thermal Impedance	θ_C < 3.5 C/W
Power Consumption	15W Max
Max Junction Temp	140C
Max Case Temp	88C

Figure 6. GPU Mechanical Characteristics

2.4.1.1. Graphics processor

The Graphics Processor consists of the transformation and lighting engine, a pixel processing pipeline, and a rasterization unit. Included with these blocks are the memory controllers, cache controllers, and logic to connect the various computational blocks. The rasterization unit outputs a digital video signal output as a parallel bit stream clocked by the pixel clock or some multiple of the pixel clock.

Refer to the *NV2A Design Specification* for a detailed description of the GPU.

2.4.1.2. Integrated North Bridge

The Integrated North Bridge functional block provides the system memory controller, P6 front-side bus interface, LDT bus interface, and the arbitration unit functionality. This block arbitrates between the CPU system bus and the GPU memory bus and processes the memory transactions to and from the unified memory pool. The Memory controller also bridges the CPU system bus to the PCI bus for interface to the peripheral logic and IO controllers.

The unified memory pool is implemented in 200MHz DDR SDRAM.

2.4.1.3. Front Side Bus Interface

The front-side bus interface to the CPU will be a P6 bus clocked at 133MHz.

2.4.1.4. LDT Bus Interface

The LDT Bus is a high-speed, low pin-count bus with dedicated upstream and downstream transfer channels. The bus is capable of combined transfers of up to 800MB/s (400MB/s up and 400MB down simultaneously).

2.4.1.5. Digital Video Interface

The digital video samples will be output to the TV encoder via a 12-bit parallel digital video interface, clocked on both edges. The output format is 4:4:4 YCrCb, 4:2:2 YCrCb, or 4:4:4 YPrPb.

The GPU shall supply HSYNC and VSYNC signals to the TV encoder, but the TV encoder shall supply the pixel clock. The GPU shall output a composite sync signal used to drive the sync output of the controller ports.

2.4.1.6. Clock Generator

The clock generator includes phase-locked loops for synthesizing the clock signals required for the various logical units, including the front-side bus to the CPU, the DDR memory busses, the LDT bus to the MCPX, and the GPU core clock. The high-level description of the clock generator is shown below:

Clock Input:

13.5MHz

Clock Outputs:

250/300MHz – GPU Core

200MHz – DDR, LDT

133MHz – CPU

2.4.2. TV Encoder

The TV Encoder takes as input digital video signals over a parallel digital interface from the GPU, and outputs analog CVBS/Y/C or Y/Pr/Pb signals. The TV Encoder section converts the analog component signals and outputs the appropriate signals to drive either a television monitor, computer monitor, or HDTV monitor, based on the settings of the configuration registers. Programming of the configuration registers is accomplished via an I^2C bus connected to the core logic chip.

The TV Encoder is capable of outputting all of the modes described in the following section, which includes:

Composite and s-Video NTSC, PAL, or SECAM

Composite PAL and Component RGB (625/50) for SCART operation

Component YPrPb 480p, 720p, or 1080i HDTV

The TV Encoder supports selective application of Macrovision anti-recording signals as follows; For NTSC and PAL output modes, Macrovision 7.01 anti-recording is applied to the composite and s-Video outputs.

The output signals are driven on to the AVIP connector by 75Ω cable driver amplifiers. Anti-alias filtering and EMI suppression filtering is accomplished via off-chip filter networks as described in detail in the AVIP section.

The following paragraphs describe the system-level specifications for the TV Encoder. A detailed description of the TV Encoder, including electrical/mechanical characteristics and software interface are described in detail in the document entitled *Flicker-Free Video Encoder with Ultrascale Technology*.

2.4.2.1. Digital Video Interface

12-bit parallel

Dual-edge clocked

1.2V signaling

H/V/Field to be supplied by the GPU CRT controller logic, Pixel CLK to be generated by the TV Encoder

2.4.2.2. Additional Features

Macrovision 7.0 or better for CVBS and Y/C outputs

Wide Screen Signaling

Copy Generation Management System

2.4.2.3. Video Input Modes

24-bit RGB

24-bit 4:4:4 YCrCb

24-bit 4:2:2 YCrCb

HDTV 4:4:4 YPrPb (SMPTE-274M, SMPTE-296M)

2.4.2.4. Video Output Modes

The television modes used by country are tabulated in Appendix C of this document. To support the countries in which Xbox is to be marketed, the TV Encoder shall support the following video output modes:

NTSC-M (CVBS + Y + C)

PAL-I (CVBS + Y + C)

PAL-I (CVBS + R/G/B)

SECAM-L (CVBS + Y + C)

HDTV (Y + Pr + Pb)

2.4.2.5. Conversion Mode Matrix

The TV Encoder shall support the following combination of input and output modes:

Frame Buffer Configuration			NTSC	PAL SECAM	HDTV		
Pix	Line	Frame (Hz)			480p	720p	1080i
640	480	59.94 Interlaced	•				
704							
720							
640	480	59.94 Progressive	•				
704							
720							
640	480	50 Progressive		•			
704							
720							
640	576	50 Interlaced		•			
704							
720							
720	480	60p			•		
1280	720	60p				•	
1920	1080	30i					•

Figure 7. Video Output Conversion Matrix

2.4.2.6. Analog Video Output Multiplexing

The TV Encoder provides four video DAC outputs. To support all the composite, s-Video, and component modes, the four outputs must be multiplexed. The DAC multiplex table is shown below:

DAC Output	SDTV Mode	SCART Mode	HDTV Mode
DACA	Y	G	Y
DACB	C	R	Pr
DACC	Not Used	B	Pb
DACD	CVBS	CVBS	Not Used

Figure 8. DAC Output Allocations

Each TV Encoder DAC output is capable of driving a single 75Ω terminated load. Passive filtering is required to minimize EMI and spectral aliases arising from the digital to analog conversion. The filter arrangements and characteristics are described in the AVIP section.

2.5. Audio Subsystem

The audio subsystem consists of an Audio Processor Unit (APU) and a digital audio interface controller. The APU and digital audio interface controller are integrated into the system core logic chip MCPX.

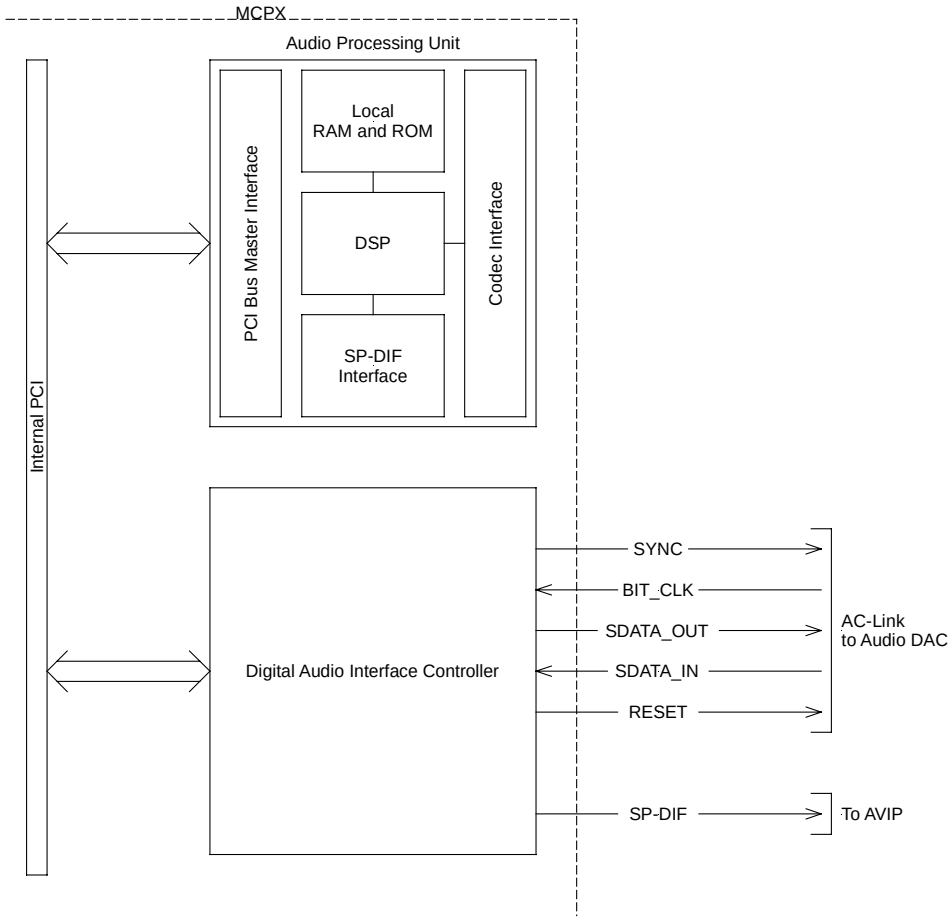


Figure 9. Audio Subsystem Block Diagram

The capabilities of the audio subsystem include:

Advanced Audio Processor – Synthesis, effects, and mixing operations are performed by a dedicated APU.

AC-Link Out – The audio subsystem shall output two-channel AC-Link audio to the audio DAC. The performance and characteristics of the DAC are described in the AVIP section..

Electrical SP-DIF Output – The audio subsystem shall provide electrical SP-DIF output for interface to an external optical SP-DIF driver. The optical SP-DIF transmitter shall be implemented as part of an AV expansion pack as described in the accessories section of this document. The SP-DIF interface may be used for stereo or AC-3 encoded 5.1 channel modes.

The detailed specification of the individual subsystem components is contained in the following sections.

2.5.1. Audio Processing Unit

The Audio Processing Unit is integrated into the core logic chip (MCPX). The APU consists of a fixed-function DSP and two programmable DSP's. The DSP's can access audio streams in system memory, have local code and data memory, and output the processed streams back to system memory for output via the AC-Link and SP-DIF interfaces.

Input Formats	Output Formats
1-18 Samples per block	1, 2, 4, 6 Samples per block
8, 16, and 32-bit containers	16 or 32-bit containers
DX8 Capabilities	
Sub-Mix Bins	
2nd Pass Processing	
2D Wave	3D Support
Direct Sound, WAVE	HRTF with Cross Talk
Per-Voice Filtering	I3DL2 Reverb
	Occlusion and Obstruction
	Near Field Affects
	Real-Time AC-3 Encode
DLS1/2 Support	Voice Support
Two envelope engines w/LFO	256 Total Hardware Voices
DLS Filtering	64 3D voices with cross over
Pan, Pitch, Vibrato, Tremolo	32 DX8 sub-mix voices with hardware sub-mixing160 2D/WT voices, all DLS2 capable
Reverb and Chorus send	20 effects and input voices

Performance

133MHz Clock frequency

Fixed-function 24-bit DSP @ 2000MIPs

Programmable-function 24-bit DSP @ 500MIPs for effects processing

Programmable-function 24-bit DSP @ 500MIPs for real-time AC-3 Encode

+85dB with 16bps inputs

24-bit sample processing paths

32-bit mixing

Figure 10. APU Feature Summary

2.5.2. Digital Audio Interface Controller

The Digital Audio Interface Controller provides the DMA engine and interface for outputting the processed audio streams to the audio outputs. The audio subsystem provides digital audio in two formats: SP-DIF and AC-Link.

The AC-Link interface is compliant with revision 2.1 of the AC-Link interface specification. The AC-Link digital audio stream is converted to an analog signal by an audio DAC. The DAC, post filtering, and audio performance characteristics are described in detail in the AVIP section.

The AC-Link drives an AC-97 audio codec that provides analog line-level audio outputs to the AVIP. The details of the digital to analog converter and related signal conditioning circuits are discussed in detail in the AVIP section.

The audio subsystem outputs a logic-level (3.3V) SP-DIF signal that is presented to the AV Interface connector. Conditioning of this signal for electrical or optical transmission via coax or optical fiber is accomplished in the AV-Pack.

The analog and digital output streams may be separate, so it is possible to output unencoded stereo via the analog interface while simultaneously outputting AC-3 encoded multi-channel audio via the SP-DIF.

Software Note:

Due to incompatibilities between pre-AC-3 digital amplifiers and current digital amplifiers, this output must be configurable such that AC-3 output can be blocked. If AC-3 encoded audio is input to a pre-AC-3 digital amplifier, the amplifier erroneously interprets the AC-3 encoding as PCM audio samples, and the result is high-level noise being fed to the speakers. There is a possibility of damage associated with this scenario, so the default configuration should be to force all digital output to be PCM.

An alternative implementation is to default the SP-DIF output to disabled, then force the user to select one mode or the other. This would reduce the chance that a user with an AC-3 compatible system would miss out by not enabling the AC-3 output mode.

2.6. Core Logic (MCPX)

The Core Logic, or Media/Communications Processor (MCPX) contains all of the core logic functions, including the audio processor and interface controller, hard disk and DVD drive interfaces, USB controllers, and system support functions. The MCPX connects to the GPU via an LDT bus that provides 800MB/s transfer rate. The individual logic blocks integrated into the MCPX core logic chip are described in the following sections.

Parameter	Min	Typical	Max	Unit
Core and LDT Power Supply V1P5 I_{V1P5} Power Consumption	1.45	1.5	1.65 TBD TBD	V A W
LVTTL Interface Power Supply V3P3 I_{V3P3} Power Consumption	3.0	3.3	3.6 TBD TBD	V A W
RTC Battery Power Supply V_{BAT} I_{BAT}	0.9	1.5	1.5 4	V µA
Total Power Consumption			2	W
Case Temperature (T_{CASE})	0		88	C

Figure 11. MCPX Electrical Characteristics

Parameter	Specification
Package	PBGA, 340 balls max at 1mm pitch, 23x23mm
Ball-Out Configuration	5 rows with 6x6 core array of power/gnd
Construction	Encapsulated die, Chip up with bond wire substrate
Substrate	TBD
Thermal Impedance	TBD
Power Dissipation	2W Max
Max Case Temp	88C

Figure 12. MCPX Mechanical Characteristics

The following sections describe the functionality of the core logic functions. Refer to the nVidia MCPX Data Sheet for a detailed description.

2.6.1. Audio Processor and Digital Audio Interface

These logic blocks are described in the Audio Subsystem description.

2.6.2. ATA Interface

The MCPX implements a single ATA-100 port with scatter-gather mastering. The master supports the following transfer modes:

PIO Mode 0, 1, 2, 3, and 4

DMA Mode 0, 1, and 2

UDMA-33, 66, and 100

The Xbox motherboard and cable assemblies will be designed only for ATA-33 operation, using the DMA-33 transfer mode.

2.6.3. USB Host Controller

The MCPX implements a USB host controller compatible with the Open Host Controller Interface (OHCI) 1.0a implementing the Universal Serial Bus protocol, version 1.1. The host controller is mapped to the four game controller ports.

The USB differential transceivers are implemented directly on the core logic IC. Power management and overcurrent protection is provided by external power management IC's. The host controller monitors the overcurrent flags from the power management circuit. The port power enable signals are controlled on each port individually by GPIO pins.

The MCPX actually implements two USB host controllers. The second host controller is unused in the production version of the Xbox, but is mapped to a fifth port on development units to provide debug information.

This port may be eliminated entirely in a future version of the MCPX chip, so it should never be utilized by an Xbox application.

2.6.4. Ethernet MAC

The Ethernet MAC features dual-speed CSMA/CD for 10 and 100 Mb/s operation as defined in IEEE 802.3u. The MAC includes a Media Independent Interface (MII) to an external PHY.

The features of the MAC include:

Provides transmit FIFO to provide frame buffering for increased system latency, automatic retransmission with no FIFO reload, automatic transmit padding, and FCS generation

Provides receive FIFO to provide frame buffering for increased system latency, automatic flushing of collision fragments, automatic receive pad stripping, and a variety of address match options

Supports Unicast, Multicast, and Broadcast addressing

Supports filtering for at least 16 multicast addresses

Offers two-part deferral algorithm

Recognizes late collision

Provides internal and external loop-back

The MII Interface Features:

Compliant with IEEE 802.3u (MII/RMII)

Supports half- and full-duplex operation

Controls and receives status from external PHY through the MII management interface

Supports auto-negotiation through the external PHY

Supports automatically polling the status of external PHY status including Link Status, Auto-negotiation ability, Half and Full Duplex ability.

2.6.5. General Purpose IO Pins

The MCPX Implements 9 General Purpose IO Pins. The GPIO pins provide software control of functions by the CPU. The GPIO pins have the following general DC characteristics. Refer to the MCPX data sheet for detailed information.

Parameter	Min	Typical	Max	Unit
Output Voltage Characteristics V_{OL} @ I_{OUT} = 4mA V_{OH} @ I_{OUT} = -1mA	 3.0		0.3	V
Input Voltage Characteristics V_{IL} V_{IH}	0.8		 2.0	V
Input Voltage Range	-0.5		5.5	V

Figure 13. GPIO DC Electrical Characteristics

The GPIO pins are mapped as tabulated below:

GPIO	Signal Name	Direction	Comment
0	FWENB	OUT	This pin is reserved to allow for in-system re-programming of the Flash-ROM in development systems only. This pin shall not be terminated in the retail version of the product.
1	VBUSENB1	OUT	These pins provide per-port control of the VBUS power enable for each of the five controller/expansion ports.
2	VBUSENB2	OUT	
3	VBUSENB3	OUT	
4	VBUSENB4	OUT	
5	VBUSENB5	OUT	This pin provides port control of the VBUS power for the fifth port. This port is only installed on development units.
6			
7			
8	LVLCNT0	OUT	These pins provide control of the SCART STATUS output of the AVIP port.
9	LVLCNT1	OUT	

Figure 14. GPIO Pin Usage

2.6.6. Internal Boot ROM

The MCPX includes a 512-byte ROM mapped to the reset vector of the CPU address space. This ROM overlaps the top 512 addresses of the external ROM.

2.6.7. External ROM Interface

The MCPX shall support addressing of up to 16MB of external Flash ROM, EEPROM, or masked ROM. The interface is implemented as a simplified X-Bus interface, with only memory read/write capability and no interrupt or DMA support.

The bus consists of the following pins:

ADDRESS[23..0] – 24 Address lines are supplied by MCPX, 21 address lines are connected on board to address up to 2M addresses.

DATA[7..0] – 8 Data lines for reading and writing data from and to the bus.

CS – A single chip select to qualify access cycles

MEMR – A memory Read qualifier signal

MEMW – A memory Write qualifier signal

Note:
Although the MCPX External ROM Interface can address up to 16MB of ROM, the motherboard design only wires 21 address bits to the ROM component. This allows up to 2MB of ROM to be installed on the motherboard, and since the upper address lines do not affect the chip select qualification, the external 2MB ROM will be aliased 8 times in the 16MB address space.

The External ROM may alternatively be interfaced to the MCPX via the LPC interface. See the note in the following section describing how to enable this interface.

2.6.8. LPC Interface

The MCPX implements an LPC interface for bridging to legacy ISA devices for development purposes or as an alternative boot ROM interface. The LPC header provides debug signals only.

The LPC interface provides an alternative means of connecting the boot ROM to the MCPX. For the first year design, the boot ROM will be accessed via the external ROM interface described previously. The motherboard shall implement an LPC header to support debugging devices to be connected for development purposes, and to aid in troubleshooting during manufacturing line rework. The process used to redirect the ROM access to the LPC interface is described in the following paragraphs.

Immediately following the rising edge of POWOK, which signals the end of the reset cycle, the MCPX reads the Dword of ROM space on the External ROM Interface at physical address 0xFF00:0000. This location in the ROM should always be programmed to contain a ‘1’ in the least-significant bit of that address. If a ROM is present on this bus, bit[0] will be read high and all future access cycles will go to the External ROM Interface.

To enable External ROM access to be directed to the LPC bus, the data bit[0] line of the External ROM Interface is tied low. When this bit is read low at RESET, all future accesses in the External ROM address space are directed to the LPC.

The LPC interface is terminated in a 16-pin debug port described in detail in the LPC Header section.

2.6.9. LDT Bus

Data transfer between the NV2A and MCPX are carried over a full-duplex Lightning Data Transport (LDT) data bus. This bus consists of two links, one serving transfers from NV2A to MCPX, and the other servicing transfers from MCPX to NV2A.

High Speed – Low Pin Count

Differential – Unidirectional Bus

800MB/s Peak (Scalable)

Efficient Pipelined Architecture for Low Latency

Support Multiple Outstanding Split Transactions

Flat/Fair Arbitration

Legacy & Non-Legacy Master Recognition

Isochronous & Asynchronous Queue

Pipeline Read & Writes

2.6.10. Clock Generator

The clock generator module in the MCPX takes as input a stable clock reference (F_{REF}) and uses multiple phase-locked loops to generate clocks for the other blocks in the MCPX. The system-level clocking architecture is described in detail later in this document.

Input Frequency:

CLK13P5

Output Frequencies:

200MHz – LDT

100MHz – LDT Bus Interface, APU Bus Interface, USB Bus Interface, Ethernet MAC, Legacy Block Bus Interface

133MHz – APU Core

48MHz – USB DPLL

33MHz – Legacy Block

2.6.11. Real Time Clock (RTC)

The MCPX implements a real time clock that may be powered by an external primary lithium coin cell. The RTC provides a real time reference for date and time of day, as well as a small amount (256 bytes) of battery-backed RAM for storage of system parameters.

The real time clock includes a 32.768 kHz oscillator, a clock and calendar timer, an alarm (which generates an interrupt when a specified time occurs), and 256 bytes of non-volatile RAM. It is register compatible with the real time clock found in the original AT design (which used the MC146818).

2.6.11.1. Power

The real time clock includes its own power plane, VRTC, which is powered by an external 1.5-volt lithium battery. An external diode network allows the RTC to power from the 3VSB standby power supply to conserve battery life when the unit is plugged into line power, but in the OFF state.

The VRTC power plane is required to not be damaged when it is not powered while the other internal power planes are powered. Conversely, it is allowed to have VRTC powered while any other planes are not powered.

2.6.11.2. Oscillator

The real time clock includes a 32.768 kHz oscillator that is used to keep time. The oscillator circuit is guaranteed to be accurate to within 10 parts per million over the external temperature and

capacitance ranges. This provides for a time loss of less than 30 seconds per month. Switching the real time clock power source between VDD_RTC and 3VSB does not affect the operation or frequency of the oscillator.

When power is initially applied to the oscillator circuit (normally through a battery connected to VDD_RTC), the oscillator circuit requires 500 milliseconds before the internal 32 kHz clock is stable. Oscillator bypass mode (described in the first section; AMD-internal only) can be used to hasten initialization for testing purposes.

2.6.11.3. Self Reset

There is no external reset signal for the logic powered by VRTC. The circuitry is required to generate its own internal reset signal when VRTC power is applied to the IC (if necessary) such that it is guaranteed to power up in a functional state. The application of VRTC power is allowed to be very noisy—rapidly going up and down—as a battery is being inserted into a socket. The self-reset signal is allowed to be up to two seconds long.

2.6.11.4. 24-Hour Rollover Restriction

If the RTC date is changed within two seconds of a day rollover on the last day of the month, undefined behavior will occur.

2.6.12. CPU Support Logic

2.6.12.1. Interrupt Controller

The MCPX implements dual Programmable Interrupt Controllers (8259) (PIC). The interrupt controllers support edge and level sensing inputs, internal interrupt routing and sharing, and PCI interrupt routing.

INTR, Output (open drain)

> INTR (Interrupt) is released (OD output) by the MCPX to signal the CPU that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.
>
> Note: INTR is used for the Frequency Strap during the reset sequence. See related section below.

The interrupt sources take varied paths from their sources to the PIC (8259). The possible sources of normal maskable interrupts (not including NMI or SMI) are:

> SCI and TCO from the ACPI / System Management block
>
> Internal USB 0 & 1 Interrupts
>
> Internal MAC 0 & 1 Interrupts
>
> Internal ACI & MCI Interrupts
>
> Internal IDE Interrupts (Typically IRQ14 & IRQ15)
>
> Internal Timer Interrupt (IRQ0)
>
> Internal RTC Interrupt (IRQ8)
>
> Internal Co-processor Interrupt (IRQ13)
>
> External LPC Serial IRQ Interrupts (Including Keyboard IRQ1)

Note: SMBus interrupts, TCO interrupts and GPIO interrupts are ORed together with the SCI interrupt in the System Management logic.

The Interrupt signals to the PIC can be either rising edge-triggered or active-low level-triggered. From a system viewpoint, only the Serial IRQ's can be edge-triggered interrupts. Traditional edge-

triggered interrupts will generate a rising edge to indicate the presence of an interrupt. Conversely, level-sensitive interrupts are asserted low to indicate one or more interrupts are present. Edge and level sensitivity must be programmed into the PIC for each interrupt via the Edge/Level Control registers.

2.6.12.2. Programmable Interval Timer

The MCPX implements a programmable interval timer compatible with the standard 8254. Refer to the 8254 data books for a detailed description. All three of the timer channels are capable of generating interrupts. Timer output signals are not provided to external pins.

The clock source for the timers is the 13.5MHz reference clock.

2.6.12.3. Legacy AT Support

The MCPX supports the AT-Legacy Register set. These signals are required for initialization of the CPU during RESET. See section 2.6.12.5 for details of how these signals are used during RESET.

NMI

NMI is used to force a non-maskable interrupt to the CPU. The MCP can generate an NMI when either SERR# from an internal or external bus is generated, IOCHK# is asserted via the Serial IRQ from LPC, or by the System Management logic. NMI is reset by setting the corresponding NMI acknowledge bit or clearing the enable/disable bit in the respective register.

Note: NMI is used for the Frequency Strap during the reset sequence.

A20M#

A20M# is not actively used in the Xbox architecture, except during RESET to initialize the CPU PLL setting.

FERR# Control and IGNNE#

The CPU asserts FERR# to indicate an error from the coprocessor. IGNNE# is only used if the coprocessor error reporting function is enabled. If FERR# is asserted, an internal IRQ13 is generated to the interrupt controller. It is also used to gate IGNNE# signal to the CPU to ensure that it is not asserted unless FERR# is active. IGNNE#, when enabled, is driven to the processor when a write is done to the Coprocessor Error Register (AT)0x00F0. IGNNE# remains asserted until FERR# is inactive. If a write is done to the Coprocessor Error Register (AT)0x00F0 when FERR# is inactive, it is ignored (IGNNE# is not asserted).

FERR# is the only input from the CPU to the MCPX. This input may be at a lower voltage level that 1.8V depending on the CPU Voltage.

Note: IGNNE# is used for the Frequency Strap during the reset sequence.

2.6.12.4. RESET Control

The CPU interface block includes logic for initializing the CPU and clearing the CPU cache. The MCPX supports a means of generating a physical CPU RESET via software control by clearing and then setting a bit in an MCPX register. Refer to Appendix G for a detailed map of the system RESET control flow and timing.

PWRGD, Input

PWRGD (Power Good) is driven from the power supply to signal that the VDD3 rail is stable. IN the Xbox implementation, PWRGD will be driven by the SMC to force the system to RESET. This is the main source of reset for much of the internal logic. PCIRST# and CPURST# are generated from this signal.

INIT#, Output
STPCLK#, Input

INIT# is asserted for 16 PCI Clocks to reset the processor. This is generated by a combination of events. The 16-clock counter for INIT# assertion will halt while STPCLK# is active. Therefore, if INIT# is supposed to go active while STPCLK# is asserted, it will actually go active after STPCLK# is de-asserted.

Causes for INIT# or CPURST# to go active:

1. Shutdown special cycle from the CPU
2. PORT92 bit[0] write, where the INIT_NOW transitions from a 0 to a 1.
3. PORTCF9 bit[1] write, where RST_CPU bit[2] was a 0 and SYS_RST bit[1] transitions from a 0 to a 1.

CPURST#, Output
PCIRST#, Output

CPURST# is used to reset the CPU and it's cache.

PCIRST# is used to reset most of the system's peripheral logic, including the LDT Bus.

2.6.12.5. CPU Speed / Frequency Strapping Control

For Intel CPUs, the MCPX directly sets the speed straps for the processor, saving external logic. The MCPX will perform the following:

1. While PCIRST# is active, the MCP drives A20M#, IGNNE#, NMI, and INTR high.
2. As soon as PWRGD goes active, the MCP read the FREQ_STRAP field contents in the RTC Power well.
3. If the power state transition is from S3, S4, S5, G3 (CPURST# required), then it will drive them to the CPU. (Note: S1 transitions to S0 do not require a CPURST# and therefore do not set the frequency strap.)

FREQ_STRAP[3:0]	Signal
[0]	NMI
[1]	INTR
[2]	IGNNE#
[3]	A20M#

The FREQ_STRAP register is in the RTC well. The value in the register can be forced to 4'b1111 by pulling AC_SDATAOUT high. Resetting the RTC well logic will also set these to 4'b1111. This setting is considered the "safe" setting.

2.6.12.6. System Management Bus Interface

The MCPX implements two clocked serial interface ports implementing the System Management Bus 2.0. This block provides a multi-master clocked serial interface for the System Management Controller and the CPU to communicate. A complete map of the SM Bus interconnection can be found in Appendix C.

2.7. System Management Controller

The System Management Controller (SMC) is a stand-alone microcontroller that performs several important system control duties. The SMC is always powered by the standby voltage output of the system power supply, so it is always active regardless of the power state of the rest of the system. The SMC communicates with the system CPU via the System Management Bus (SMBus) port on the south bridge. The duties of the SMC include the following:

System power supply control

System RESET

Temperature monitoring and fan control

Front panel IO monitoring (POWER, RESET, and INDICATORS)

AVIP Mode monitoring

DVD Control

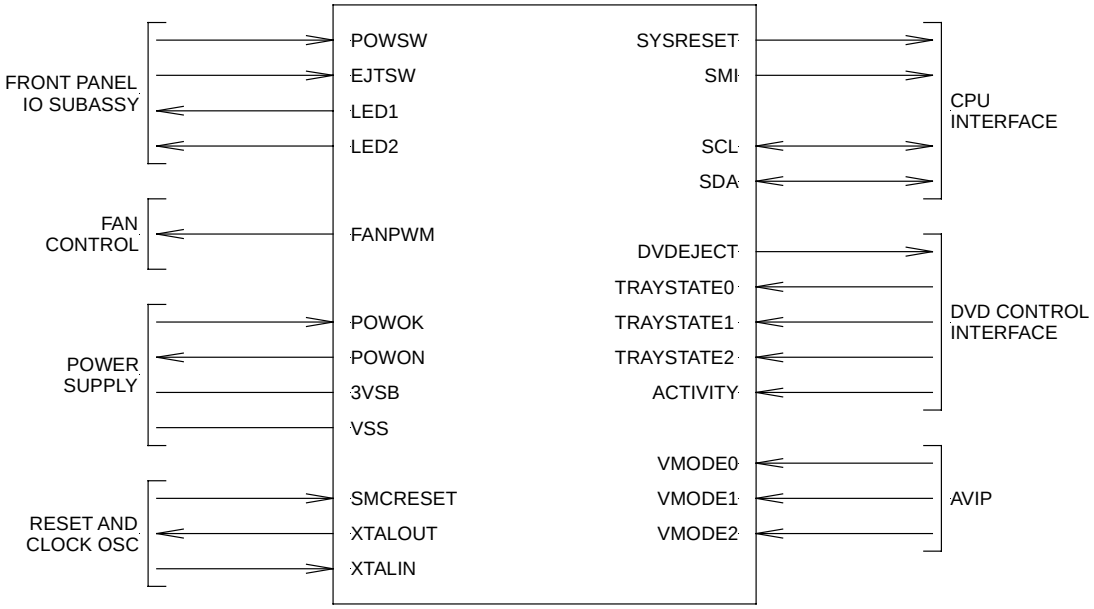


Figure 15. SMC IO Diagram

The SMC communicates with the CPU through the SMBus protocol. The command set for the SMC and the state diagrams defining its behavior are described in detail in the *System Management Controller Firmware Specification*. Refer to Appendix C for the SM Bus addresses for reading from and writing to the SMC via SM Bus.

2.7.1. Pin Out

The SMC microcontroller is specified as the Microchip PIC16LCR63T-10/SO. Refer to the Microchip PIC16C63 data sheet for detailed specifications of this chip. The table below defines the pin usage in this application:

Pin	Signal Name	Direction	PIC16C63	Comment
1	SMCRESET#	IN	MCLR/Vpp	Pull up to 3VSB via 4.7k
2	LED1	OUT	RA0/AN0	LED1 Cathode (Red), active high
3	LED2	OUT	RA1/AN1	LED2 Cathode (Green), active high
4	SYSRESET#	OUT	RA2/AN2	Drives the PWRGD to MCP./CPU (0 = reset, 1 = not reset)
5	EJTSW	IN	RA3/AN3/Vref	Eject Switch Input (0 = switch pressed, 1 = not pressed)
6	SMI	OD_OUT	RA4/TOCKI (OD out)	SMI output to CPU
7	DVDEJECT	OUT	RA5/SS/AN4	Eject control to DVD (0=open tray, 1=close tray)
8	VSS	POWER	VSS	System Ground
9	XTALIN	PASSIVE	OSC1/CLKIN	Connect to crystal or ceramic resonator
10	XTALOUT	PASSIVE	OSC2/CLKOUT	Connect to crystal or ceramic resonator
11	AUD_CLAMP	OUT	RC0/T1OSO/T1CKI	Mutes audio when driven high
12	POWOK	IN	RC1/T1OSI/CCP2	Asserted when power supply is stable (0=power not good; 1=power is good)
13	FANPWM	OUT	RC2/CCP1	PWM output for fan speed control
14	SCL	BIDIR	RC3/SCK/SCL	SMBus Clock
15	SDA	BIDIR	RC4/SDI/SDA	SMBus Data
16	POWON	OUT	RC5/SDO	Controls power supply (0=power off, 1=power on)
17	SPARE	OUT	RC6/TX/CK	Used as a test output
18	POWSW	IN	RC7/RX/DT	Power Switch Input (0 = switch pressed, 1 = not pressed)
19	VSS	POWER	VSS	System Ground
20	3VSB	POWER	VDD	Connect to 3.3V Standby
21	SPARE	IN/OUT	RB0/INT	
22	VMODE0	IN	RB1	Video mode input from AVIP
23	VMODE1	IN	RB2	Video mode input from AVIP
24	VMODE2	IN	RB3	Video mode input from AVIP
25	TRAYSTATE0	IN	RB4	Tray state from DVD
26	TRAYSTATE1	IN	RB5	Tray state from DVD
27	TRAYSTATE2	IN	RB6	Tray state from DVD
28	ACTIVITY	IN	RB7	Activity indicator from DVD

Figure 16. SMC Pin Out

This section describes the system management controller and the support circuits. The state diagrams are described in greater detail in the *SMC Firmware Specification*.

2.7.2. Power Control

The SMC monitors the front-panel POWER switch and controls the system power in a predictable and reliable manner. The behavior of the POWER switch is to toggle the power state of the system

between the ON and OFF states, regardless of the status of the CPU. In the event of a CPU crash, it is necessary to force the power off state without further intervention from the user.

In a normal system shutdown (i.e. the CPU is not crashed, but the user has decided to shut down the application) the SMC notifies the CPU of the power OFF event, and the CPU is allotted time to acknowledge the event and perform any shutdown procedures required, such as completing disk write operations. The shutdown should be transparent to the user, who should experience the video screen going blank (i.e. no signal output), audio going quiet, and the power indicator light extinguishing.

Refer to Appendix G for the system reset flow map. This appendix describes the reset sequence controlled by the SMC.

2.7.3. Temperature Monitoring

The SMC shall monitor the CPU die temperature and the internal ambient air temperature in one location of the chassis. Temperature sensing is implemented by use of a dedicated temperature sense IC. This IC measures the CPU die temperature by connecting to the on-chip temperature sense diode, and can also measure the temperature of its own die by utilizing an internal temperature sense diode. The figure below shows the internal architecture of this sensor IC and how it is connected to the system. Refer to Appendix C for the SM Bus map and addresses.

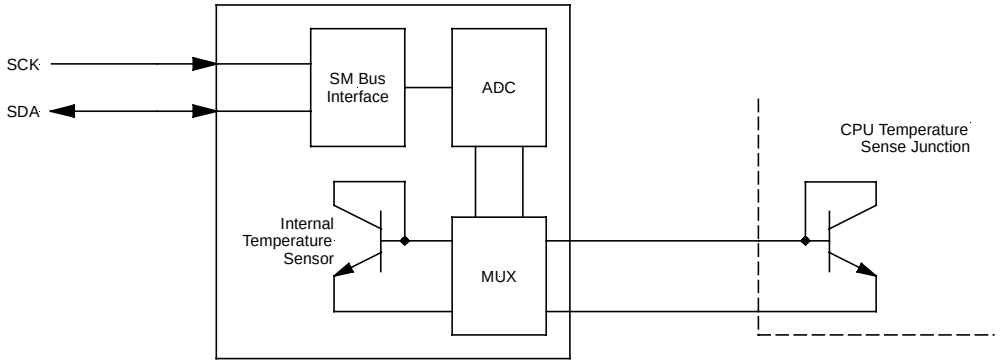


Figure 17. Temperature Monitoring Circuit

As shown above, the temperature sensor measures the temperature of the CPU die by using a dedicated diode junction provided for this purpose. The IC is physically located on the motherboard in such a way that its internal temperature sensor correlates to the internal ambient air temperature.

The IC specified for this function is the Analog Devices ADM1032ARM. Refer to the *ADM1032 Data Sheet* for detailed description of this part.

2.7.4. Fan Control

The SMC monitors the system temperature and controls the speed of the system fan in accordance with the measured temperatures.

The SMC communicates with a temperature sensor IC to monitor system temperature. There are two temperature sensors on the motherboard, providing measurement capability of the CPU junction temperature and the internal air temperature in the vicinity of the sensor chip. This capability is described in the previous section.

The System PSU has an automatic thermal overload shutdown circuit. In the event of thermal overload in the power supply, the SPS will shut off system power. The SMC will see POWOK go false. There is no way to determine whether POWOK went low due to this thermal condition or whether a brownout condition exists on the line voltage.

For the motherboard sensors, the SMC will compare the temperature readings (averaged) to three setpoints. Two setpoints are used for hysteresis and will tell the SMC to increase or decrease the fan speed. The third setpoint is for thermal overload. In a thermal overload condition, the SMC will immediately put the system in reset, turn the fan to its maximum speed, flash the LEDs to indicate thermal overload, wait until the system is back within its safe operating range, and then shut off.

Fan speed control is accomplished by pulse-width modulation as shown in the circuit below. Note that the speed of the fan is proportional to 1 minus the duty cycle of the PWM. To turn the fan off, the FANPWM output should be asserted high with 100% duty cycle. For the lowest speed, the fan is driven with the maximum duty cycle shown in the table, maximum speed is achieved with 0% duty cycle.

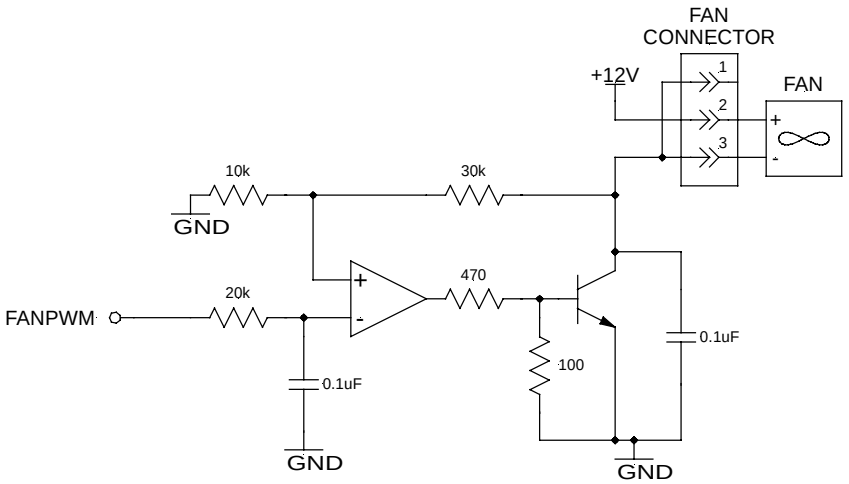


Figure 18. Fan Speed Control Circuit

Parameter	Min	Typical	Max	Unit
DC Current			400	mA
Fan Voltage	4		12	V
PWM Frequency	100		1000	Hz
PWM Duty Cycle (High Time/Period) Maximum Operational Speed Minimum Operational Speed Stop	0	 100	 56 	%
Voltage Ripple			10	%

Figure 19. Fan Speed Control Circuit Design Parameters

Note:

Fan speed control design parameters shall be defined after EVT and thermal solution testing.

2.7.5. Front Panel IO

The SMC is responsible for driving the front-panel indicator LED. The indicator is implemented as a red/green bicolor LED, which is capable of being illuminated RED, GREEN, or ORANGE (red/green). The CPU may override the state of the indicator by issuing commands via the SMBus, with the exception of the thermal overheat and power off states.

The schematic below shows the interconnection of the FPIO components with the SMC. The input circuits provide series impedance to protect the SMC from electrostatic discharge.

The bicolor LEDs are in a common cathode configuration, making it necessary to ground the common cathode and source current to the two anodes individually. The schematic diagram shows the bias resistor and driving transistor arrangement.

The details of the transistor bias networks and LED series resistor values are to be determined pending final UI and industrial design.

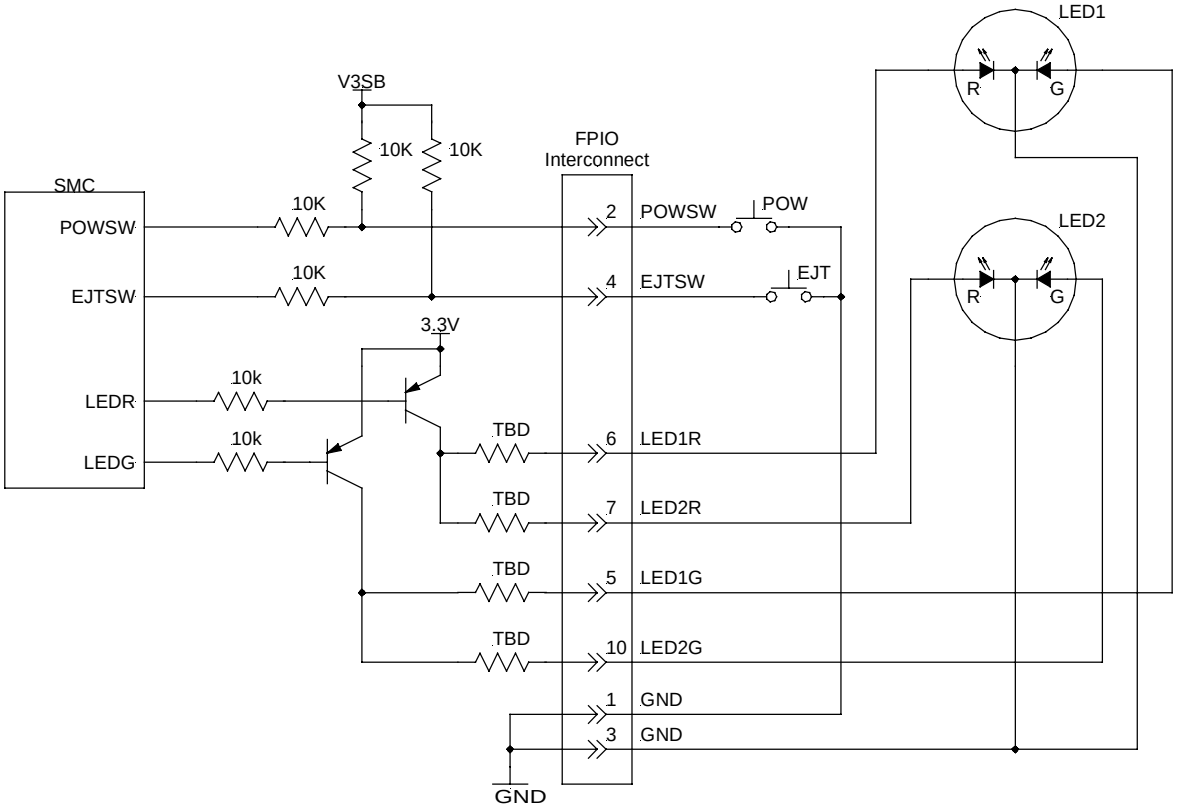


Figure 20. Front Panel IO Schematic

The front panel LEDs are automatically controlled by the SMC under most circumstances, until the XOS transfers control to the application. At that point, the application may select the LED mode via API calls to XOS, unless an exception condition occurs. The general behavior of the LEDs is diagrammed in the flow chart below, but the detailed control is incorporated into the detailed state machine descriptions in the *SMC Firmware Specification*.

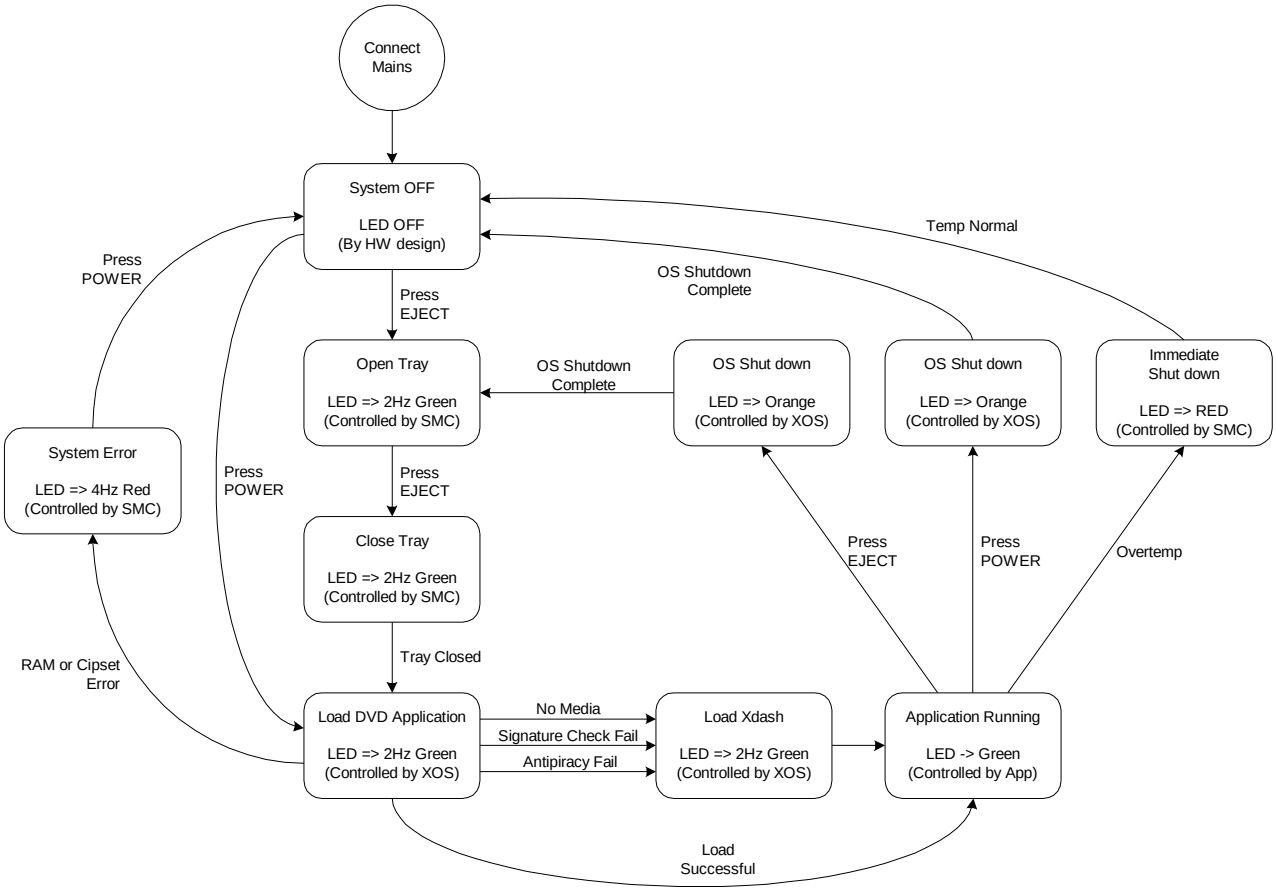


Figure 21. LED Behavior Flow Chart

As shown in the flow diagram, the system initially enters the power OFF state upon connection to mains power. In this mode the LEDs are both OFF. Upon pressing either EJECT or POWER, the Xbox immediately begins to flash the LEDs GREEN. The XOS will launch either the application on the DVD or the internal Xdash application, but once the application is running, the light will transition to the solid GREEN state, unless overridden by the application through API calls to the XOS.

If the application is terminated by the user either by pressing the EJECT or POWER switch, the LED immediately goes to the blinking ORANGE state until the XOS completes any shutdown activity required.

If the Xbox overheats, the LEDs go to the blinking RED state until the system has dropped to a safe temperature, then the Xbox will automatically go to the power OFF state. If an error is detected during the boot procedure, such as RAM error, chipset error, or hardware error, the LED indicates the error by blinking RED as shown.

2.7.6. AV Mode Detect

The SMC monitors the AVIP MODE inputs and will notify the CPU (via SMI) whenever a new AV Pack is detected. The SMC will not recognize a transition to the NO PACK state as a change, but will only recognize changes between different configurations. This will allow the AV pack to be disconnected and reconnected without requiring the system to modify its output configuration. A new AV Pack is one of the three cases that cause an SMI to be sent to the CPU.

2.7.7. DVD Tray Control

The SMC is responsible for monitoring the DVD TRAYSTATE lines. This is used for two purposes: The SMC must be capable of ejecting the DVD tray (independent of the CPU), and the SMC must monitor whenever new media (CD/DVD) is placed in the drive. Any time the SMC detects that the DVD tray has been opened and then closed, it will notify the CPU of this event (via SMI). The tray closing is the third case that causes an SMI to be sent to the CPU.

2.8. System Clocking

The Xbox clocking system consists of several clocks. A block diagram of the system clocking requirements is shown in the figure below. In addition to the clock frequencies shown in the diagram, the CPU, GPU, MCPX, and TV Encoder each contain phase-locked loops to synthesize the clocks used by internal logic.

2.8.1. System Clocking Architecture

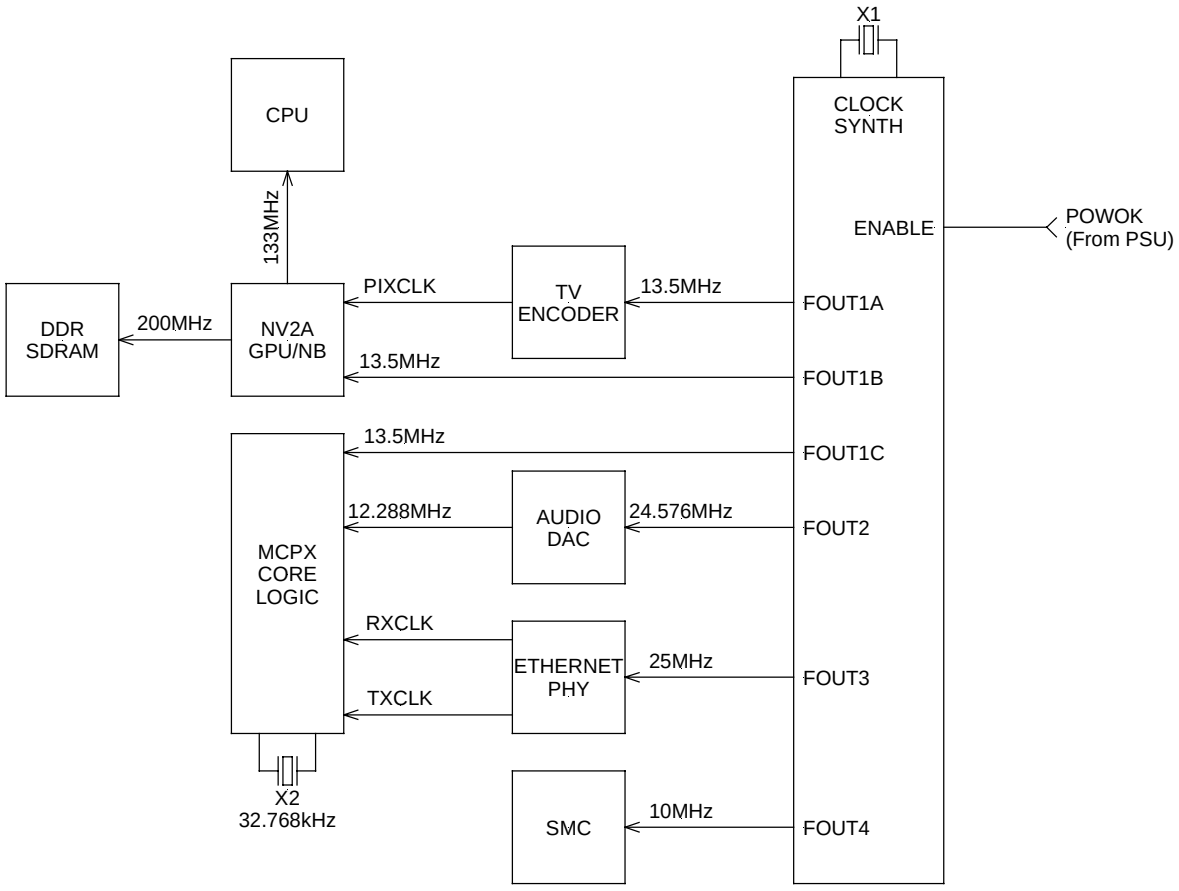


Figure 22. Clocking Block Diagram

CPU Clocking – The CPU contains a phase-locked loop to synthesize the internal core frequency as described in the CPU data sheet. The typical operating frequency for the CPU will be 733MHz.

NV2A Clocking – The GPU contains two phase-locked loops for internal clock generation. One PLL synthesizes the core clock (250-300MHz) while a second synthesizes 800MHz that is then

divided down to generate the 133MHz CPU FSB clock, the 200MHz DDR memory clock, and the LDT interface to the MCPX. The PLL's are referenced to the 13.5MHz input clock. The CRTC logic of the GPU is slaved to the PIXCLK generated by the TV Encoder. This clock will vary in frequency depending on the video mode being output.

DDR Clocking – The DDR memory clock is synthesized by the NV2A internal PLL.

MCPX Clocking – The MCPX includes several PLL's to generate the internal clocks, including the USB clock (48MHz), the ATA interface clock (66MHz), the LDT interface clock (100MHz and 200MHz), and the legacy block clock (33MHz). The PLL's and the legacy block timers are referenced to the 13.5MHz input clock. The MII interface is slaved to the 25MHz clock input, this clock is transmitted from the PHY to the MCPX as RXCLK and TXCLK. The AC-Link and SP-DIF interfaces are referenced to the 12.288MHz clock provided by the audio DAC. Lastly, the RTC block is clocked by an internal oscillator driven by an external 32.768kHz crystal.

TV Encoder – The TV Encoder inputs a 13.5MHz reference clock from the Clock Synthesizer block. A buffered version of the 13.5MHz clock is passed on to the MCPX clock to use as a reference for its internal PLL's. An internal PLL is used to generate the clocks required for video output and pixel data clocking. The TV Encoder outputs the pixel clock to the NV2A GPU. The TV Encoder requires a 13.5MHz clock with 25ppm accuracy in order to meet requirements for NTSC and PAL color encoding.

Audio DAC – The Audio DAC inputs a 24.576MHz reference clock from the Clock Synthesizer block. The reference clock is internally divided by two and output to the MCPX as a 12.288MHz clock for audio, clocking both the AC-Link audio stream and the SP-DIF audio stream. The audio clock must exhibit zero long-term frequency error compared to the video clock.

Ethernet PHY – The Ethernet PHY inputs a 25MHz reference clock from the Clock Synthesizer block. The PHY drives two 25MHz clocks into the MCPX. The Ethernet PHY requires an absolute frequency error of 100ppm maximum.

SMC – The SMC is clocked from a 10MHz PLL from the clock synthesizer.

Clock Generator ENABLE – All of the clock generator outputs, except the one that clocks the SMC, are enabled through a single ENABLE input. This signal is derived from the PSU POWOK output. The SMC enables the system PSU, which in turn should assert POWOK once the voltages have stabilized. When POWOK is not asserted (i.e. held LOW), all outputs except the SMC clock (FOUT1) are stuck at a low level.

2.8.2. Clock Generator

The clock synthesizer consists of a reference oscillator, driven by 27MHz crystal, and two phase-locked loops. Three outputs, driven through a divide by 2 prescaler, are used to output the reference clock to three destinations; the TV Encoder, MCPX, and NV2A.

The PLL's generate clocks for the Audio, Ethernet, and SMC. One PLL generates the Audio clock, which shall be derived from the following ratio: FOUT2 = 2048/1125 * 13.5MHz. This ratio results in a zero ppm relative error between the audio and video clocks. A second PLL generates the 25MHz and 10MHz outputs, by generating an intermediate frequency of 50MHz FOUT34 = 100/27 * 13.5MHz, and dividing by 2 for FOUT3 and dividing by 5 for FOUT4.

The pin out table provides for independent power supply pins for the reference oscillator and output pins, for the audio clock PLL, and for the Ethernet/SMC PLL(s). These power pins are partitioned so as to minimize jitter on the FOUT1 pins.

The synthesizer also includes an ENABLE pin which when deasserted shuts down FOUT1, 2, and 3, but leaves the SMC clock (FOUT4) running. The shutdown outputs must stick in the logic "low" state. Note that the reference oscillator must continue to operate; only the output drivers are disabled.

The notes below are referred to in the AC characteristics table that follow in the next paragraphs:

1. This specification is provided for reference only. The controlling specifications are the clock high and low times.
2. Time measured from the rising edge crossing V_{OH} to the falling edge crossing V_{OL}.
3. Time measured from the falling edge crossing V_{OL} to the rising edge crossing V_{OH}.
4. The absolute difference in period between any two consecutive clock cycles.
5. Time measured from 10% to 90% points on the rising or falling edge of the waveform.
6. Rise and fall time is measured at the clock input being driven, and may be achieved with suitable series resistance introduced between the clock output driver and the clock input.

2.8.2.1. Reference Crystal Specification

Parameter	Min	Typical	Max	Unit
X1 Fundamental Frequency		13.5		MHz
Initial Tolerance (T_A = 10-70C)			±10	ppm
Aging			±2	ppm/year

The reference crystal specification is designed to guarantee a total frequency error of ±25ppm over temperature, over the life of the product.

2.8.2.2. FOUT1A/B/C Reference Clock Output Specifications

Parameter	Min	Typical	Max	Unit
Frequency		13.5		MHz
Duty Cycle [1]	45	50	55	%
Clock High Time [2]	33		41	ns
Clock Low Time [3]	33		41	ns
Clock to Clock Jitter [4] Peak to Peak RMS			 300 50	ps
Load Capacitance	2		7	pF
Rise/Fall Time [5, 6] C_L = 2pF C_L = 4pF	 500		 3000	ps

2.8.2.3. FOUT2 Audio Clock Output Specifications

Parameter	Min	Typical	Max	Unit
Frequency		24.576		MHz
Synthesis Error (relative to Reference Frequency)			0	ppm
Duty Cycle [1]	45	50	55	%
Clock High Time [2]	18.3		22.4	ns
Clock Low Time [3]	18.3		22.4	ns
Clock to Clock Jitter (RMS) [4]			300	ps
Load Capacitance		10		pF
Rise/Fall Time (C_L = 10pF) [5, 6]	1		4	ns

2.8.2.4. FOUT3 Ethernet Clock Output Specifications

Parameter	Min	Typical	Max	Unit
Frequency		25		MHz
Synthesis Error (relative to Reference Frequency)			0	ppm
Duty Cycle [1]	35	50	65	%
Clock High Time [2]	14		26	ns
Clock Low Time [3]	14		26	ns
Clock to Clock Jitter (RMS) [4]			300	ps
Load Capacitance		3		pF
Rise/Fall Time (C_L = 3pF) [5, 6]	1		4	ns

2.8.2.5. FOUT4 SMC Clock Output Specifications

Parameter	Min	Typical	Max	Unit
Frequency		10		MHz
Synthesis Error (relative to Reference Frequency)			0	ppm
Duty Cycle [1]	25	50	75	%
Clock High Time [2]	25		75	ns
Clock Low Time [3]	25		75	ns
Load Capacitance		15		pF
Rise/Fall Time (C_L = 15pF) [5, 6]			15	ns

2.8.3. RTC Clock Specifications

Parameter	Min	Typical	Max	Unit
X2 Fundamental Frequency		32.768		kHz
Frequency Tolerance			25	ppm

2.9. Digital Versatile Disk (DVD) Drive

The DVD drive will be used for loading of content and applications. The DVD must be capable of reading DVD disks, CD Audio disks, and CD-ROM disks. The DVD drive shall not be capable of reading CD-Recordable (CD-R) media.

The drive incorporates a tray loading mechanism operated electrically. The tray open and close control line is driven by the SMC in accordance with user input via the EJECT switch, and the SMC state machine described in the SMC firmware specification.

The DVD Drive interfaces to the CPU through an AT-Attachment (ATA) Interface shared with the hard disk drive. The DVD Drive is configured as a slave device, the HDD is configured as the master. The ATA interface shall operate in UDMA-33 mode.

The DVD Drive is described in detail in the *DVD-ROM Drive Specification*. The following sections are provided for system-level design considerations only.

2.9.1. Media Compatibility

The drive is compatible with both 8cm and 12cm standard media. The drive shall be capable of addressing the Burst-Cutting area of DVD media disks.

Non-Standard Media: Rectangular media based on the removal of material from a standard 8cm disk is allowed, so long as the following restrictions are observed. The shape must be both statically and dynamically balanced about the center of the disk. The width and length of the disk must not fall below the dimensions shown in the drawing below. The media format for this form factor may be CD-ROM or single-layer DVD.

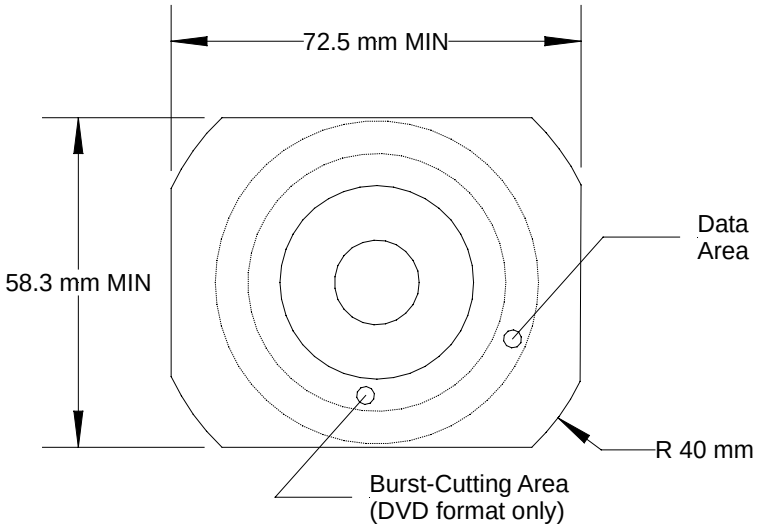


Figure 23. Rectangular Optical Disk Media

2.9.2. Format Compatibility

- Single-Layer, Single or Dual Sided, 12cm DVD-ROM (DVD-5 and DVD-10) manufactured in accordance with ECMA-267, 120mm DVD-Read-Only Disk.
- Dual-Layer, Single or Dual Sided, 12cm DVD-ROM (DVD-9 and DVD-18) manufactured in accordance with ECMA-267, 120mm DVD-Read-Only Disk.
- Single-Layer, Single Sided, 8cm DVD-ROM manufactured in accordance with ECMA-268, 80mm DVD Read-Only Disk.
- Dual-Layer, Single Sided, 8cm DVD-ROM manufactured in accordance with ECMA-268, 80mm DVD Read-Only Disk.
- CD-ROM XA (Yellow Book)
- CD-DA (Red Book)

Note:

DVD-RAM and CD-RW compatibility are specified here to support the development of applications only. DVD-RAM and CD-RW compatibility is not guaranteed on units sold in retail channels.

- Single-Layer DVD-R of type TBD by DVD drive manufacturer.
- CD-RW (Read mode only)

2.9.3. Spindle Speed Control

The drive shall operate at Constant Angular Velocity (CAV) in both CD and DVD formats. CAV operation results in streaming speeds in the range of 2-4.8x for 12cm DVD, and 6.4 to 16x for 12cm CD. The spindle velocity shall be selectable under software control, which may select one of three speeds:

High Speed: This speed corresponds to approximately 3000rpm, depending on the drive implementation, and results in the maximum DVD and CD read rates shown in the performance specification table.

Medium Speed: This speed corresponds to approximately 2000rpm. An application may select this speed to minimize acoustic noise, or the OS may select this speed automatically in response to a read error.

Low Speed: This speed corresponds to approximately 1000rpm, and represents the slowest speed that the drive may be operated in. This speed will result in lowest power dissipation and lowest acoustic noise in the system, especially when reading rectangular media.

2.9.4. Performance Specifications

For the purposes of this specification, the following definitions apply:

Access Time – The time that elapses between an ATAPI command to read data from the disk and when the first data is transferred via the ATA interface. For practical purposes, this time includes the ATAPI command transit time, seek time, rotational latency, read/ECC time, and ATA data transit time.

Average Access Time – This represents the average time required to access data from the disk. This performance metric shall be measured by the following profile- the seek shall originate on any track on the disk to a track 1/3 of a stroke away; the seeks shall include an equal number of inner to outer and outer to inner seeks; the tool shall accumulate a minimum of 200 seeks and compute the

average by dividing the total amount of time required to perform the test by the number of seeks performed.

Full Stroke Access Time – The access time for a seek that originates in the vicinity of the innermost track, to the outermost track, or from the outermost track to the innermost track. This performance metric shall be measured by making subsequent inner to outer and outer to inner accesses, accumulating a minimum of 200 seeks, and dividing the total time elapsed by the number of seeks performed.

Startup Time – The time elapsed between the tray close and the first drive being ready to complete the first data transfer request. This metric shall be measured using the standard test disk. The time shall be measured from the point at which the tray reaches the “closed” position, and shall include the spindle startup time; the media detection and laser calibration time; and the read of the DVD-ROM root directly.

Launch Time – The time elapsed between the tray close and the first 64MB launch file being transferred from the disk. This specification is provided for reference only, as an indication of the time required to launch a typical application from DVD. The actual time required to launch an application will vary depending on the physical location of the launch file, the exact size of the file, and the quality of the DVD media.

This metric shall be measured using the standard test disk, containing a 64MB file located near the vicinity of the outermost track on the disk. The time shall be measured from the point at which the tray reaches the “closed” position, and shall include the Startup Time (as defined above); the time required to seek to the launch file; and the transfer of the complete 64MB launch file.

Sustained Data Rate – The rate at which data may be read continuously from the disk and transferred via the ATA interface, averaged over a large data file located on contiguous physical tracks. The time shall be measured between the first ATAPI command to read data following a seek command, to the final data being transferred. The rate shall be computed by dividing the size of the data file and dividing by the time elapsed.

Parameter	Min	Typical	Max	Unit
Reference Streaming Speed 1x DVD 1x CD-ROM Mode 1 1x CD-ROM Mode 2 1x CD-DA		 11.08 1.23 1.40 1.41		Mbps
CAV rotational velocity Single Layer DVD Dual Layer DVD All CD formats	 1148 1148 1148		 2870 3160 3160	rpm
Relative DVD Streaming Speed (read only, CAV) 12cm Media 8cm Media Rectangular Media	 2x 2x 2x		 5x 3.3x	
Sustained DVD Data Rate 12cm DVD Media 8cm DVD Media Rectangular DVD Media	 22.16 22.16 22.16		 55.40 36.56 TBD	Mbps
Relative CD Streaming Speed (read only, CAV) 12cm Media 8cm Media Rectangular Media	 6.4x 6.4x 6.4x		 16x 9x	
Sustained CD Data Rate 12cm CD-ROM Mode 1 12cm CD-ROM Mode 2 12cm CD-DA 8cm CD-ROM Mode 1 8cm CD-ROM Mode 2 8cm CD-DA Rectangular Media	 7.87 8.96 9.02 7.87 8.96 9.02 TBD		 19.68 22.40 22.56 11.07 12.60 12.69	Mbps
Average Access Time (1/3 stroke, at max angular velocity) CD DVD-5 DVD-9		 100 130 130		ms
Full-Stroke Access Time (1/3 stroke, at max angular vel) CD DVD-5 DVD-9		 300 300 300		ms

Figure 24. DVD Data Access Performance Specifications

Note:

*The access and streaming data rates specified here represent **average** performance as defined earlier in this section. Actual access time for any particular access may be faster or slower than the specified average depending on the location of the head, the target location requested, the condition of the media, and any external vibration or shock input.*

Throughout the life of the Xbox product, the DVD drive may undergo design changes for cost reduction. These design changes may result in different performance for particular accesses, but the same average performance will be met.

Software developers should avoid depending on the timing of the DVD access in their applications.

Parameter	Min	Typical	Max	Unit
Startup Time (This parameter is to be minimized) DVD-5 DVD-9		 8 8	 TBD TBD	sec
Launch Time (This specification is provided for reference) DVD-5 or DVD-9		 18		sec
Spin-down Time			8	sec
Time to restart from Idle			5	sec
Tray Open/Close Time			4	sec
Laser auto-shutdown time		15		sec
Laser recovery time (recovery from shut down)			700	ms
Read error timeout		2		sec

Figure 25. DVD System Timing Specifications

2.9.5. Electrical Specifications

The electrical interface shall consist of two ports, including an ANSI ATAPI compatible interface port and an auxiliary power and loader control interface.

2.9.5.1. ATA/ATAPI Electrical Interface

The ATAPI interface shall operate over an ATA-33 physical interface. The ATA interface connector shall be a 40-pin header with 2.54mm center-to-center pin spacing, conforming to ANSI SFF 8059.

The ATA interface utilizes 3.3V signaling. The interface must support DMA Multiword modes 0-3, and DMA-33. PIO mode 0 is also required. The pin-out of the ATA interface is shown in the table below:

Pin	Function	Pin	Function
1	RESET#	2	GND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	KEY (no pin on header)
21	DMARQ	22	GND
23	DIOW#	24	GND
25	DIOR#	26	GND
27	IORDY	28	NOT USED (CABLE SELECT)
29	DACK1#	30	GND
31	INTRQ	32	IOCS16#
33	DA1	34	PDIAG#
35	DA0	36	DA2
37	CS1FX#	38	CS3FX#
39	DASP#	40	GND

Figure 26. ATA Interface Connector Pin Out

The DVD drive is configured as a Slave device on the ATA port. The drive supports standard ATAPI commands as described in the Software Requirements section of this document, as well as the specified special-purpose commands.

2.9.5.2. Power and Control Interface

12VDC power and the loader control/status interface shall be implemented on a secondary multi-pin connector. The interface shall include the following signals (Note signal directions are with respect to the drive):

Pin	Signal Name	Direction	Comment
1	12VDC	POWER	12VDC for motor control
2	5VDC	POWER	5VDC for digital logic
3	GND	POWER	Signal and DC current return
4	EJECT	IN	Logic level control, when asserted LOW, tray is ejected. When de-asserted (OPEN or HIGH) tray is closed.
5	TRAYSTATE0	OUT	The combined states of these signals indicate the current state of the tray and media as defined in the state diagram below.
6	TRAYSTATE1	OUT	
7	TRAYSTATE2	OUT	
8	ACTIVITY	OUT	Asserted LOW when disc activity (seek or data transfer) occurs.
9	12VDC	POWER	12VDC for motor control
10	5VDC	POWER	5VDC for digital logic
11	GND	POWER	Signal and DC current return
12	GND	POWER	Signal and DC current return

Figure 27. DVD Power and Control Interface Connector Pin Out

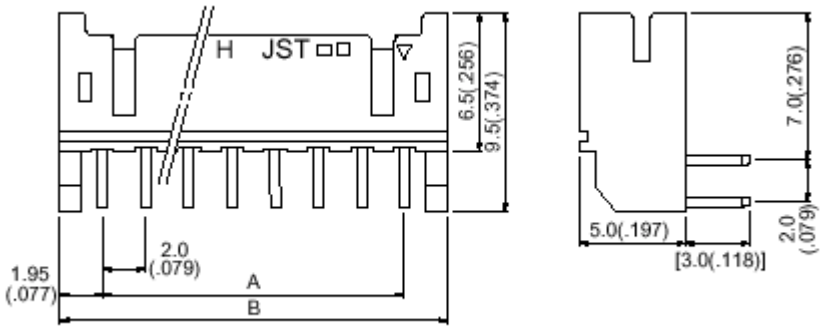
Note:

The table above describes the pin out of the DVD Power/Control Interface on the DVD drive itself. This port is connected to the motherboard via a cable assembly. The mating connector on the motherboard has two extra pins to allow for a missing pin key. Refer to the system Integration section for details of connector pin outs and cabling.

Parameter	Min	Typical	Max	Unit
Logic Supply Voltage (V_{CC5})	4.75	5.00	5.25	V
Logic Supply Current Seek Read Pause (Spinning, no data access)		 800 650	1000	mA
Motor Supply Voltage	10.8	12.0	13.2	V
Motor Supply Current Seek Read Pause (Spinning, no data access)		 600 400	1300	mA
Input Logic Level (ATA bus, control, and state outputs) Voltage Input, Low (V_{IL}) Voltage Input, High (V_{IH})	 0.0 2.0		 0.8 V_{CC5}	V
Output Logic Level (ATA bus, control, and state outputs) Voltage Output, Low (V_{OL}) @ 300µA Voltage Output, High (V_{OH}) @ 300µA	 0.0 2.7		 0.6 V_{CC5}	V

Figure 28. DVD Drive DC Electrical Characteristics

The connector type shall be JST part number S12B-PHDSS, as shown in the drawing below. Pin one is designated with a triangular marking on the connector shell. When viewing the connector from the component side of the PCB, odd numbered pins are on the top side of the connector, while even numbered pins are on the bottom side.



A= 10.0 mm, B=13.9mm

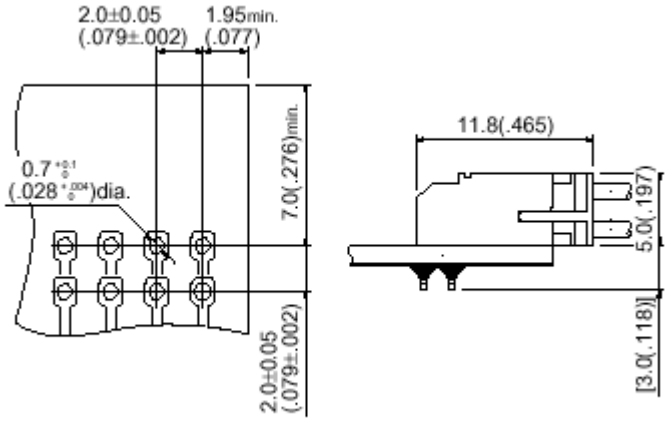


Figure 29. DVD Power and Control Interface Connector

2.9.6. Functional Requirements

2.9.6.1. Tray State Outputs

The Power and Control interface includes three state bits that are driven by the DVD drive to indicate the current state of the DVD mechanism. The state diagram below defines the state transitions and the inputs or conditions that trigger changes between states.

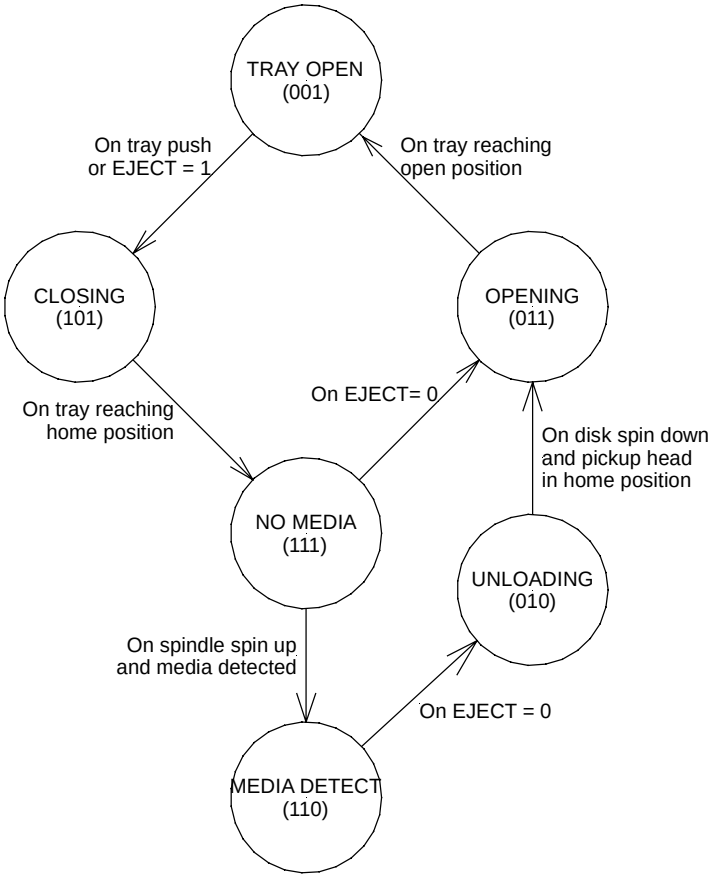


Figure 30. DVD Mechanism State Diagram

State Definitions:

TRAY OPEN – This state indicates the disk tray is fully open.

CLOSING – This state indicates the tray is the process of closing. Note that if this state is entered by a manual push on the tray by the user, that the state of the EJECT control line must be changed to prevent the tray proceeding from the NO MEDIA state directly to the OPENING STATE.

NO MEDIA – This state indicates the disk tray has closed, and the drive is attempting to detect if media is present. If no media is inserted in the drive, the drive remains in this state until ejected by EJECT=0.

MEDIA DETECT – This state indicates that the tray has closed and the valid media has been detect in the drive.

UNLOADING – This is a temporary state entered upon EJECT=0 that persists until the tray begins to open.

OPENING – This state indicates the tray is being opened.

2.9.6.2. Power Up Initialization

Upon power up, and following the initialization of the control logic in the DVD drive, the tray state outputs shall reflect the current state of the tray. If the tray state is unknown at power up, the state shall default to the CLOSING state, and transition to the correct state within 100ms. Due to this

initialization requirement, the traystate outputs should be considered invalid until 100ms after power-up.

2.9.7. Software Requirements

2.9.7.1. ATA Commands for ATAPI DVD-ROM Devices

0xA1 ATAPI Identify Device

0xA0 ATAPI Packet Command

0x08 ATAPI Soft Reset

0xE5 Check Power Mode

0x90 Execute Device Diagnostics

0xEC Identify Device

0xE1 Idle Immediate

0x00 NOP

0xEF Set Features

0xE6 Sleep

0xE0 Standby Immediate

2.9.7.2. ATAPI Packet Commands

0x4A Get Event/Status Notification

0x12 Inquiry

0xBD Mechanism Status

0x55 Mode Select(10)

0x5A Mode Sense(10)

0x1E Prevent/Allow Media Removal

0x28 Read(10)

0xA8 Read(12)

0xBE Read CD

0x25 Read Capacity

0xB9 Read CD MSF

0xAD Read DVD Structure

0x43 Read TOC/PMA/ATIP

0xA4 Report Key

0x03 Request Sense

0x2B Seek(10)

0xA3 Send Key

0x00 Test Unit Ready

2.9.7.3. Xbox-Specific ATAPI Commands

0x Set Speed

2.9.8. Mechanical Specifications

Refer to the DVD-ROM Drive Design Specification for details on the mechanical specification of the DVD drive. The following points represent a summary of specifications relevant at the system level:

The loading system shall be a standard front-loading tray designed for horizontal operation, within a maximum tilt angle 10° from the horizontal plane.

The drive shall include a tray eject actuator, accessible via a pinhole in the front panel, to release the tray mechanism in the case of a drive failure.

The tray shall automatically close when pushed manually.

2.9.9. Environmental Requirements

Parameter	Min	Typical	Max	Unit
Ambient Air Temperature	0		60	C
Non-Operational Drop Shock, 2ms pulse duration			100	G
Acoustic Sound Power L_W (A) Measured while tray opens/closes Measured while Disk is spinning at max velocity Measured in anechoic chamber with background noise level at least 10dBA below the expected measured level			 33 30	dB

2.10. Hard Disk Drive (HDD)

The hard disk drive is specified for lowest cost with suitable reliability for the console application. The expectations is that the lowest-cost configurations for the hard disk is a single-platter, single head, in a standard 3.5” form factor. The capacity of the HDD is optimized for cost, and is not required to increase over time, so the specified capacity in the table represents the minimum capacity desired. The final revision of this document shall specify the actual capacity of the HDD.

The two hard drives selected for Xbox in year one product will be:

- Seagate ST310211A
- Western Digital WD100EB

These drives meet the minimum performance requirements outlined in the following sections. The specified performance parameters represent the baseline requirement for all future Xbox hard disk drives. Due to technological and manufacturing advances, the performance of the drives is expected to vary from year to year, but the basic specifications outlined here must continue to be met.

2.10.1. General Specifications

Form Factor – Standard 3.5” form factor per ANSI specification SFF-8300. This requirement is for year one designs only. Future product iterations and cost reductions may make use of a hard disk drive in a smaller form factor.

Capacity – The capacity shall be representative of the state of the art for a single platter and single head disk drive in the first year of production. The capacity of the drive shall be no less than 10GB. The final revision of this specification shall specify the minimum drive capacity.

Electrical Interface – The electrical interface shall at a minimum conform to the ATA-2 interface standard (ANSI NCITS 317-1998). The interface connector shall be a 40-pin ATA header with 100mil center-to-center pin spacing per ANSI SFF-8059.

Command Set – The interface must support DMA Multiword modes 0-3, DMA-33. PIO modes 0-2 may be supported but are not required. The drive shall also support SMART self-test diagnostic features.

2.10.2. Performance Requirements

Parameter	Min	Typical	Max	Unit
Startup Time From Power ON to Drive Ready From Standby to Drive Ready		 8 6	 12 12	sec
Spin-down Time From Standby Command From Power OFF		 6 12	 15 30	sec
Startup Time (Power ON to Drive Ready) Seagate WD		 10 4	 8	sec
Spin-down time Seagate WD		 4 4	 8 	sec
Random Seek/Read Time		8	15	ms
Random Seek/Write Time		12	16	ms
Full-Stroke Seek Time		18	30	ms
Track to Track Seek Time		2		ms
Data Transfer Rate, Sustained	12			MB/s
Acoustic Sound Power L_W (A) Measured in anechoic chamber with background noise level at least 10dBA below the expected measured level		3.1	3.7	Bel

Note:

*The access times specified here represent **average** performance as defined earlier in this section. Actual access time for any particular access may be faster or slower than the specified average depending on the location of the head, the target location requested, the condition of the media, and any external vibration or shock input.*

Throughout the life of the Xbox product, the HDD may undergo design changes for cost reduction. These design changes may result in different performance for particular accesses, but the same average performance will be met or exceeded. The speed of the drive will most likely increase in future years.

Software developers should avoid depending on the timing of the HDD access in their applications.

2.10.3. Electrical Requirements

Parameter	Min	Typical	Max	Unit
Logic Supply Voltage	4.75	5.00	5.25	V
Logic Supply Current Peak Seeking Idle or Read		 550 500	600	mA
Motor Supply Voltage	10.8	12.0	13.2	V
Motor Supply Current Peak Seeking Idle or Read		 750 250	2000	mA

2.10.4. Environment Requirements

Parameter	Min	Typical	Max	Unit
Ambient Air Temperature	0		70	C
Non-Operational Drop Shock, 2ms pulse duration			300	G
Acoustic Sound Power L_W (A) Measured while performing random seeking ops Measured while spinning Measured in anechoic chamber with background noise level at least 10dBA below the expected measured level			 33 30	dB

2.11. Network Interface

The network interface port is compatible with IEEE 802.3 operating at 10Mbps and 100Mbps. The physical interface to Category 5 (100Mbps) and Category 3 (10Mbps) operation is implemented with a single-chip Ethernet transceiver, an isolation transformer, and associated passive components.

2.11.1. Ethernet PHY

The requirements for the Ethernet Transceiver are as follows:

- 10Mbps (IEEE 802.3) and 100Mbps (IEEE 802.3u) with Auto Negotiation
- 3.3V supply voltage and interface
- Automatic polarity detection and correction of RX channel
- Full-Duplex operation
- Media Independent Interface (MII)

The Ethernet transceiver selected for Xbox is the Level One LXT972LC.

The LXT972 is an IEEE compliant Fast Ethernet PHY Transceiver that directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs).

The LXT972 supports full-duplex operation at 10 Mbps and 100 Mbps. Its operating condition can be set using auto-negotiation, parallel detection, or manual control.

The LXT972 is fabricated with an advanced CMOS.

The features of the LXT972 are:

- 3.3V Operation
- Low power consumption (300 mW typical)
- 10BASE-T and 100BASE-TX using a single RJ-45 connection
- Supports auto-negotiation and parallel detection
- MII interface with extended register capability.
- Robust baseline wander correction performance.
- Standard CSMA/CD or full-duplex operation
- Configurable via MDIO serial port or hardware control pins
- Integrated, programmable LED drivers
- 64-pin Low-profile Quad Flat Package (LQFP)

A block diagram for the PHY is shown in the figure below:

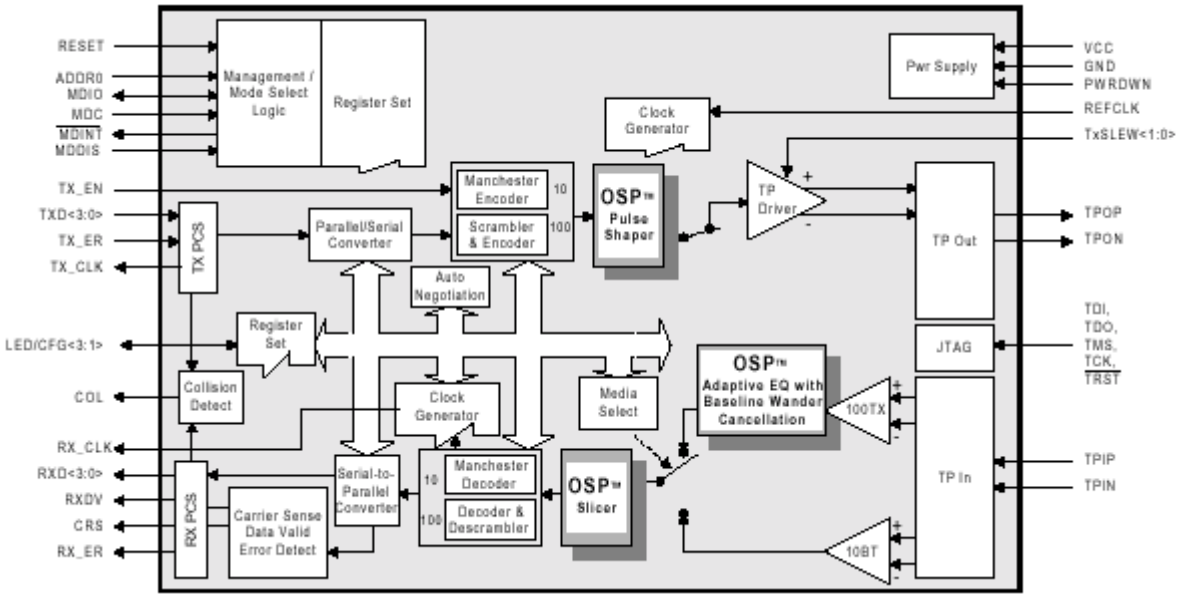


Figure 31. Ethernet PHY Block Diagram

2.11.2. Magnetics Specification

Xbox will utilize an integrated Ethernet RJ-45 connector with magnetics and LED indicators. The general specifications of the magnetic aspect of this component are shown below:

Parameter	Min	Typical	Max	Unit
Rx Turns Ratio		1:1		
Tx Turns Ratio		1:1		
Insertion Loss	0.0	0.6	1.1	dB
Primary Inductance	350			µH
Transformer Isolation		1.5		kV
Differential to Common Mode Rejection 0.1 to 60 MHz 60 to 100 MHz	 40 35			dB
Return Loss 30MHz 80MHz	 -16 -10			dB

2.11.3. Network Connector

The connector is mounted at a right angle to the PCBA. The RJ-45 connector is presented in a tab-up orientation (tab away from the PCB side). Two LED's, one on either side, are integrated in to the connector body. The green LED, visible to the left of the tab release, shall be controlled to illuminate when a network connection is established, and will blink when there is activity on the line. The yellow LED, visible to the right of the tab release, shall be illuminated if the connection is established at 100Mbps and shall not be illuminated if connected at 10Mbps.

The table below specifies the pin out of the RJ-45 Network Connector:

Pin	Signal Name	Direction	Comment
1	TPOP	OUT	Transmitter, positive phase
2	TPON	OUT	Transmitter, negative phase
3	TPIP	IN	Receiver, positive phase
4	Termination	Passive	
5	Termination	Passive	
6	TPIN	IN	Receiver, negative phase
7	Termination	Passive	
8	Termination	Passive	

Figure 32. Network Connector Pin Out

The parts qualified for this design are:

- Pulse J1026F01P
- Stewart SI50023

Note:

Final qualification will occur at DVT, the vendors and part numbers shown above may change at that time based on DVT test results.

2.11.4. Interface Circuit

The circuit below shows the interconnection of the LXT972 Ethernet PHY and the RJ-45 connector, magnetics, coupling network, and status LED's.

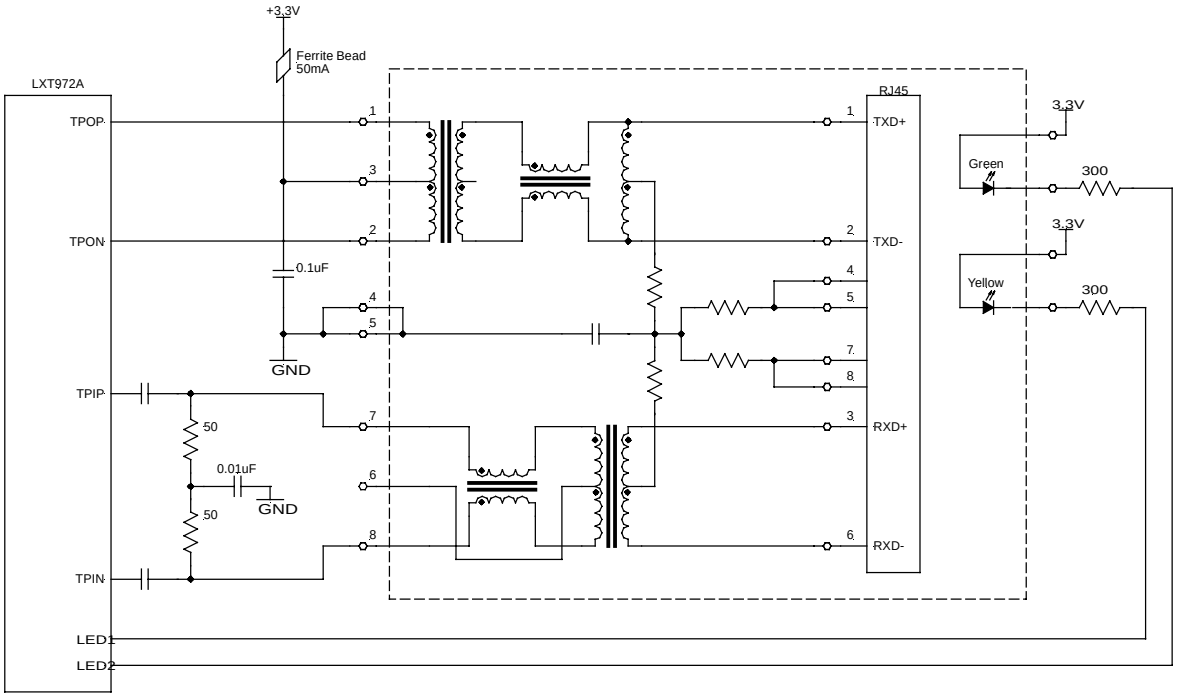


Figure 33. Ethernet PHY Interface Circuit

2.12. Audio Video Interface Port (AVIP)

The Xbox provides all audio and video signals on a single multi-pin AV connector referred to throughout this document as the AVIP. The AVIP provides all four video output signals, status signal for SCART, stereo line-level audio outputs, SP-DIF digital audio output, and the VMODE inputs.

An AV pack is connected to the AVIP to break out the signals for interconnection to a television and or audio system. By asserting the states of the VMODE control inputs, an AV pack identifies what type of television signals should be generated, and whether the audio output should be stereo or mono.

2.12.1. Mechanical Connector Characteristics

The AVIP connector consists of 24 pins total, organized as two rows of 12 conductors each with odd numbered pins on one side of the connector and even numbered pins on the other. The pins carry power, video, audio, and some logic-level input and output signals. The DCOUT and DCRETURN pins are located at the far ends of the connector. The mechanical design of the connector is such that the DCOUT and DCRETURN contacts are guaranteed to make contact before any signal pin.

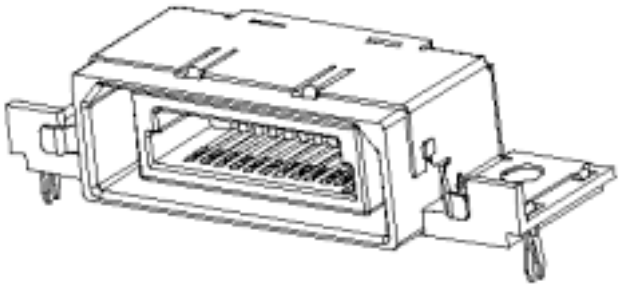


Figure 34. AVIP Mechanical Sketch Output

Pin	Signal Name	Direction	Comment
1	DCOUT	OUT	The output of this pin provides a current-limited DC power supply for active AV Pack circuitry.
2	LINE OUT (R)	OUT	This pin outputs line-level Right channel linear audio.
3	LINE OUT (L)	OUT	This pin outputs line-level Left channel linear audio.
4	GND	-	This ground is provided for connection to the Right channel audio cable shield.
5	GND	-	This ground is provided for connection to the Left channel audio cable shield.
6	SPDIF	OUT	This pin is the SP-DIF logic-level output.
7	HSYNC	OUT	Horizontal Sync Signal used for VGA output mode
8	VSYNC	OUT	Vertical Sync Signal used for VGA output mode
9	MODE1	IN	Video output mode select pin 1
10	GND	-	This pin provides a convenient grounding point for the MODE1 input if needed.
11	MODE2	IN	Video output mode select pin 2
12	GND	-	This pin provides a convenient grounding point for the MODE2 inputs if needed.
13	MODE3	IN	Video output mode select pin 3
14	GND	-	This pin provides a convenient grounding point for the MODE3 inputs if needed.
15	STATUS	OUT	SCART Status Pin
16	GND	-	Ground connection for pin 18 (Pb)
17	GND	-	Ground connection for pin 19 (C/Pr)
18	Pb B	OUT	This pin outputs the Pb component signal in HDTV mode, and the BLUE component signal in RGB SCART mode.
19	C Pr R	OUT	This pin outputs the Chroma signal in SDTV mode, and the Pr component signal in HDTV mode, and the RED component signal in RGB SCART mode.
20	GND	-	Ground connection for pin 22 (Y)
21	GND	-	Ground connection for pin 23 (CVBS)
22	Y G	OUT	This pin outputs the Luma signal in both SDTV and HDTV modes, and the GREEN component signal in RGB SCART mode.
23	CVBS	OUT	This pin is dedicated to the Composite Video Out (CVBS) in SDTV mode. In HDTV mode, this pin is not used.
24	DCRETURN	-	This pin is specifically designated to carry the DC return current.

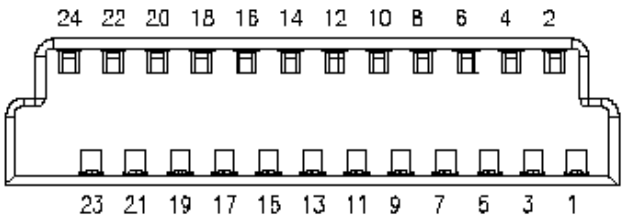


Figure 35. AVIP Connector Pin Out

2.12.2. DC Power Output

The AVIP DCOUT pin supplies 5V power to the AV Pack if needed. The output of the AVIP is short-circuit protected internally by a positive temperature coefficient thermistor. The design of the short-circuit protection circuit shall guarantee the DC output voltage range specified over the entire load current range and over the entire operating temperature range.

Parameter	Min	Typical	Max	Unit
DCOUT Voltage	4.70	5.00	5.25	V
DCOUT Current			250	mA

Figure 36. AVIP DCOUT Output Characteristics

2.12.3. Mode Selection Inputs

The AVIP supports several output configurations. The MODE inputs to the AVIP are provided to identify the type of signals expected by the AV Pack. The output mode is identified by jumper wires between the mode select pins (MODE1, MODE2, and MODE3) and GND pins on the AVIP connector as shown in the table below.

The state of these inputs is continuously monitored by the system management controller, and communicated to the Xbox OS. Changes in the state trigger notification to the OS that the AV mode has changed.

The state of these pins does not directly control the video or audio mode; the OS configures the CRT controller of the GPU and the TV Encoder through software. It is possible to configure these independently of the MODE state pins, as may be required for test purposes.

AVIP Mode Input (Pin)			Video Mode	AVIP Video Output (Pin)			
M[0] (9)	M[1] (11)	M[2] (13)		(23)	(22)	(19)	(18)
OPEN	OPEN	OPEN	No AV Pack Present	-	-	-	-
OPEN	OPEN	GND	525/60 RFU Mode (NTSC, mono audio)	$CVBS_{NTSC}$	Y_{NTSC}	C_{NTSC}	-
OPEN	GND	OPEN	625/50 RFU Mode (PAL/SECAM, with mono audio)	$CVBS_{PAL}$	Y_{PAL}	C_{PAL}	-
OPEN	GND	GND	HDTV Mode (Y/Pr/Pb)	-	Y	Pr	Pb
GND	OPEN	OPEN	525/60 SDTV Mode (NTSC)	$CVBS_{NTSC}$	Y_{NTSC}	C_{NTSC}	-
GND	OPEN	GND	VGA	-	G	R	B
GND	GND	OPEN	625/50 SDTV Mode (PAL-I)	$CVBS_{PAL}$	-	-	-
GND	GND	GND	625/50 SDTV Mode (PAL-I) SCART	$CVBS_{PAL}$ Y_{PAL} -	- - G	- C_{PAL} R	- - B

Figure 37. Video Mode definitions

2.12.4. Digital Audio Output

The AVIP provides a logic-level SP-DIF signal for digital audio interfaces. The SP-DIF output is a 3.3V logic swing, and must be electrically or optically conditioned to implement a standard IEC-

60958 interface. This function is implemented in the Enhanced AV Packs by use of an optical transmitter module, such as Toshiba TOTX-178A.

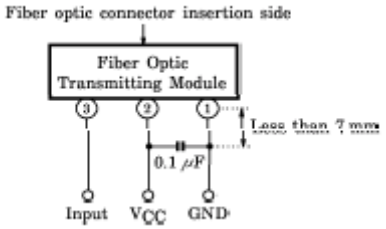


Figure 38. SP-DIF Optical Transmitter Module

2.12.5. Analog Audio Output

The analog audio output is a circuit comprised of an audio DAC, filter/amplifier, and coupling network. The figure below describes the interconnection of the various components. The MCPX provides the digital audio stream via the AC-Link interface to the audio DAC. The audio DAC is implemented as a simplified AC-97 CODEC that features only stereo output, without mixer or volume control features.

The clock source the system is the 24.576MHz output of the clock generator chip. The DAC provides clocking for the AC-Link interface. The SMC drives a clamp control line that, when used in conjunction with the power supply POWON and the AC-Link nRESET signal, provides a means of power up and down the system with minimal “pop” being generated by the audio circuits.

The filter/amplifier is a simple Operational Amplifier stage that provides a second-order low pass response and additional voltage gain to meet the output level requirements. The coupling network provides DC blocking and ESD protection for the active circuitry.

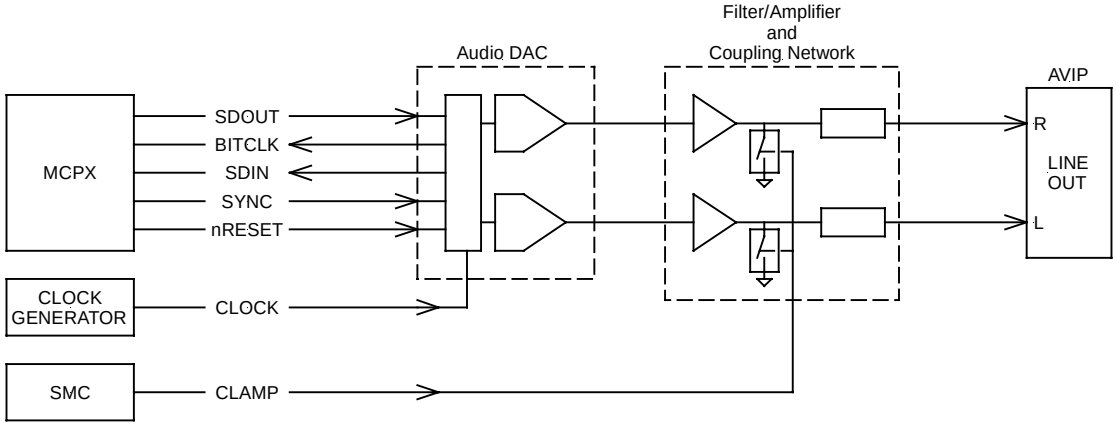


Figure 39. Analog Audio Block Diagram

2.12.5.1. Performance Requirements

The analog audio output shall be designed to IEC-61938 specifications for analog audio interface impedances and levels. In addition, the analog audio path shall be designed to meet the performance requirements of Dolby Surround and AC-3 decode certification. In addition, the system shall be designed to minimize “pop” when power is cycled. The performance requirements to achieve this certification are summarized below:

Parameter	Min	Typical	Max	Unit
Full Scale Output Voltage (1kHz tone at 0dBFS) (note 1)			2.0	V_{RMS}
Inter-channel Relative Phase Mismatch (notes 2, 3)			5	°
Inter-channel Output Level Mismatch (note 3)			0.5	dB
Dynamic Range (note 4)	85			dB
Passband Frequency	20		20k	Hz
Passband Frequency Response (note 5)	-1.0		+0.5	dB
Frequency Response (-3dB)		22		kHz
Total Harmonic Distortion and Noise (THD+N) (note 6)			0.1	%
Channel Separation (note 6)	80			dB
Signal to Noise Ratio (SNR)	85			dB
Output Impedance (note 7)	20	TBD	2200	Ω

Figure 40. Analog Audio Output Performance Specifications

Note 1: Measured while outputting a 1kHz tone at 0dBFS. According to Dolby specifications, fixed-level outputs must not exceed this level under any output condition.

Note 2: All outputs must maintain absolute polarity and the same phase relationship between channels as the original input signals as specified.

Note 3: Measured with –20dBFS signal output on both channels

Note 4: Measured relative to a 0dBFS signal, using CCIR-2k weighting and an average responding meter

Note 5: Measured relative to a –10dBFS input signal over the entire passband frequency range.

Note 6: Measured relative to a 0dBFS signal

Note 7: Line outputs to be capacitively coupled

2.12.5.2. Audio DAC Requirements

The audio DAC provides the conversion of the AC-Link audio stream to an analog signal. The DAC is implemented as a simplified stereo AC-97 CODEC, with the mixer, volume controls, analog inputs, and analog to digital conversion functions eliminated. The AC-Link interface is 3.3V logic, and is compliant with AC-97 v1.03. The clock (24.576MHz) is provided by the system clock generator. For detailed specifications, refer to the WM9709 Data Sheet.

2.12.5.3. Filter Network Requirements

The audio filter and coupling network performs additional analog signal conditioning to meet the remaining audio output requirements as listed below:

Filtering – The Filter provides attenuation of out-of band noise generated by the sampling aliases, and high-frequency noise coupled from the high-speed digital electronics in the rest of the system.

Amplification – The DAC output is limited to 1 V_{RMS} peak output. The filter network provides a gain of 2 so that the output is capable of 2 V_{RMS} peak output.

DC Elimination – The DAC output and filter output are DC biased due to the use of unipolar power supplies. The coupling capacitor provides blocking of the DC component.

ESD Isolation – The series resistance and associated capacitance provide protection from ESD events coupled directly to the audio output pin.

Power On Transient Suppression – The FET switch provides a means of controlling the discharge of the DC voltage across the coupling capacitor, preventing the output from emitting a “pop” during power up/down events. The system shall allow 200ms from RESET for the anti-pop circuits to stabilize before the first audio signals are generated.

2.12.6. Video Outputs

The analog video outputs are driven by a television encoder, which is driven by the digital video interface of the GPU. The television encoder converts the digital video to composite NTSC/PAL, component s-Video, component RGB, and component HDTV television signals.

The TV encoder has four DAC outputs. These four outputs are multiplexed between the three main modes of operation, SDTV, SCART, and HDTV. In SDTV mode, the DACs must output CVBS, Y, and C to support Composite and s-Video outputs. In SCART Mode, the DACs must output CVBS, and RGB component signals. In HDTV mode, the DACs must output Y, Pr, and Pb signals.

Since the analog filtering requirements for SDTV and HDTV outputs differ in terms of frequency cutoff and DAC sample rate, two filter response characteristics are required. This is most easily accomplished by implementing the SDTV filters in the SDTV AV Packs, and cascading them with the higher-bandwidth HDTV filters. To minimize cost, one of the four DAC outputs is dedicated to CVBS, allowing its accompanying SDTV filter to be implemented on the motherboard.

The sections that follow describe the filter arrangements for each of the modes in detail.

2.12.6.1. SDTV Mode

The SDTV Mode includes two video outputs: Composite (CVBS) and s-Video (Y/C). The CVBS, Y, and C signals are output simultaneously on individual pins of the AVIP connector, each capable of driving a single 75Ω back-terminated transmission line. This mode applies to the Standard NTSC, Standard PAL, and Standard SCART AV packs. The Enhanced SCART AV Pack, which supports component RGB output, is described in the next section.

DAC D of the TV Encoder is dedicated to the CVBS output, and so the accompanying filter is implemented directly on the motherboard. A standard NTSC, PAL, or SCART AV Packs only supports composite video output, so this can be implemented with a simple cable.

Enhanced AV Packs support s-Video, and so require Y and C outputs in addition to the CVBS output. The Y and C outputs for s-Video share the same DAC outputs as two of the HDTV signals, and so, the filters for these outputs are implemented in the AV Pack PCBA, and are cascaded with the HDTV filters implemented on the motherboard.

The figure below shows how the filters are arranged in the Xbox and AV Pack to implement the SDTV mode.

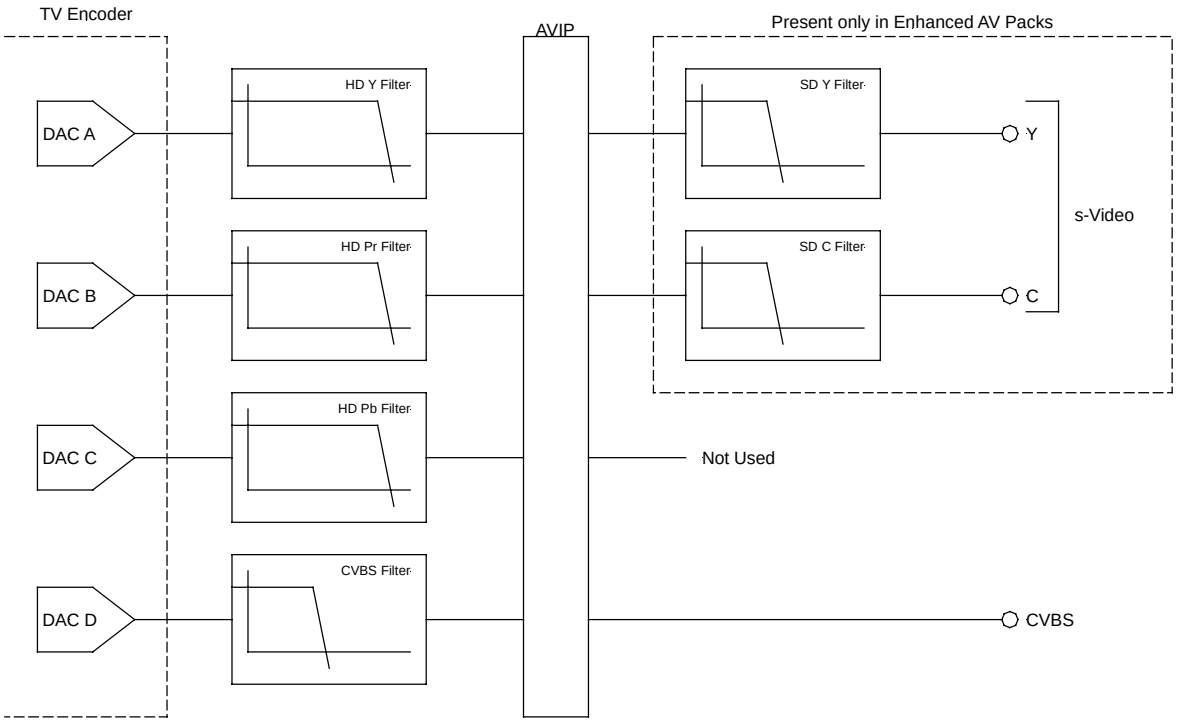


Figure 41. Video Filter Arrangement, SDTV Mode

The filter below is implemented on the motherboard and outputs CVBS to the AVIP. The performance of this filter is shown in the table that follows.

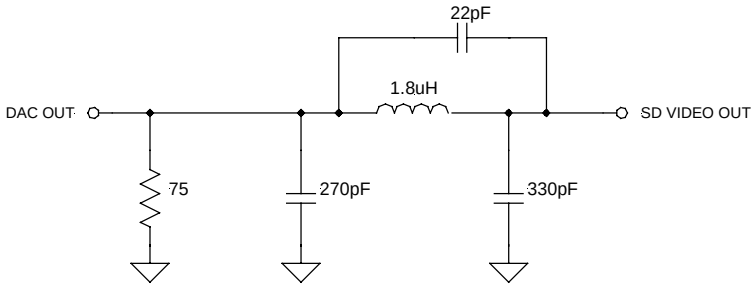


Figure 42. CVBS Filter Circuit

The filters used for the component s-video outputs consist of two stages. The first stage is the HDTV filter implemented on the motherboard, the second stage is the filter implemented in the AV Pack. The filter performance shown in the table describes the transfer function of the two filters in cascade (i.e. from DAC OUT to SD VIDEO OUT.)

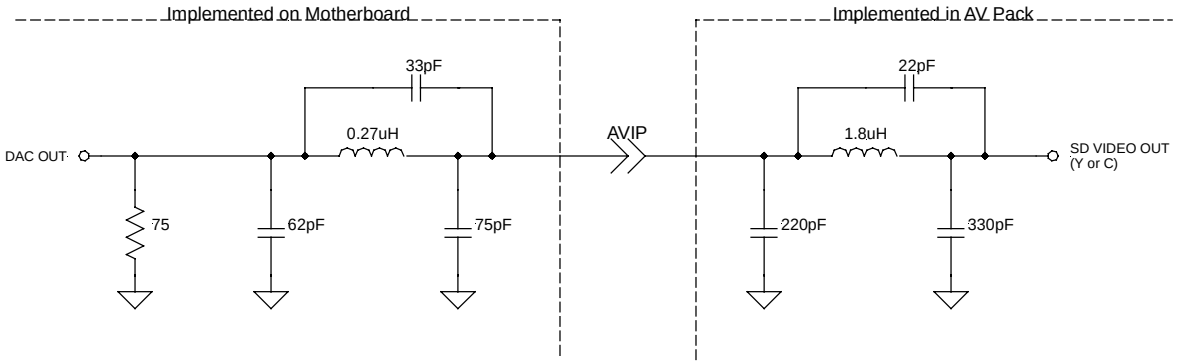


Figure 43. SD (Y and C) Filter Circuit

Parameter	Min	Typical	Max	Unit
CVBS Filter				
F_{LO} (-3dB)			0	MHz
F_{HI} (-3dB)	6			MHz
Attenuation @ 8MHz	60			dB
SDTV Y and C Filter				
F_{LO} (-3dB)			0	MHz
F_{HI} (-3dB)	6			MHz
Attenuation @ 8MHz	60			dB

Figure 44. Analog Video Filter Architecture, SDTV Mode

2.12.6.2. Enhanced SCART Mode

The SCART interface provides four video signals that can be configured to be composite video and component RGB (CVBS+RGB), or s-Video (Y/C). The Xbox OS can select either mode when the Enhanced SCART AV Pack is connected to the Xbox.

In the CVBS+RGB configuration, the CVBS, R, G, and B signals are output simultaneously on individual pins of the AVIP connector, each capable of driving a single 75Ω back-terminated transmission line.

In the Y/C mode, the Y and C signals are driven on the appropriate pins. The two remaining pins that would normally carry B and G signals are driven with the Y waveform.

In addition to the video outputs, an additional pin drives the aspect ratio selection pin on the SCART connector. This pin is set to one of three voltage levels to indicate the format of the output video signals in SCART mode. The details of this output circuit are described in a later section.

DAC A is dedicated to the CVBS output, and so the accompanying filter is implemented directly on the motherboard. The R, G, and B outputs are cascaded filters identical to that described in the previous SDTV Mode section. Refer to that section for filter characteristics.

The figure below shows how the filters are arranged in the Xbox and attached AV Pack to implement the Enhanced SCART mode.

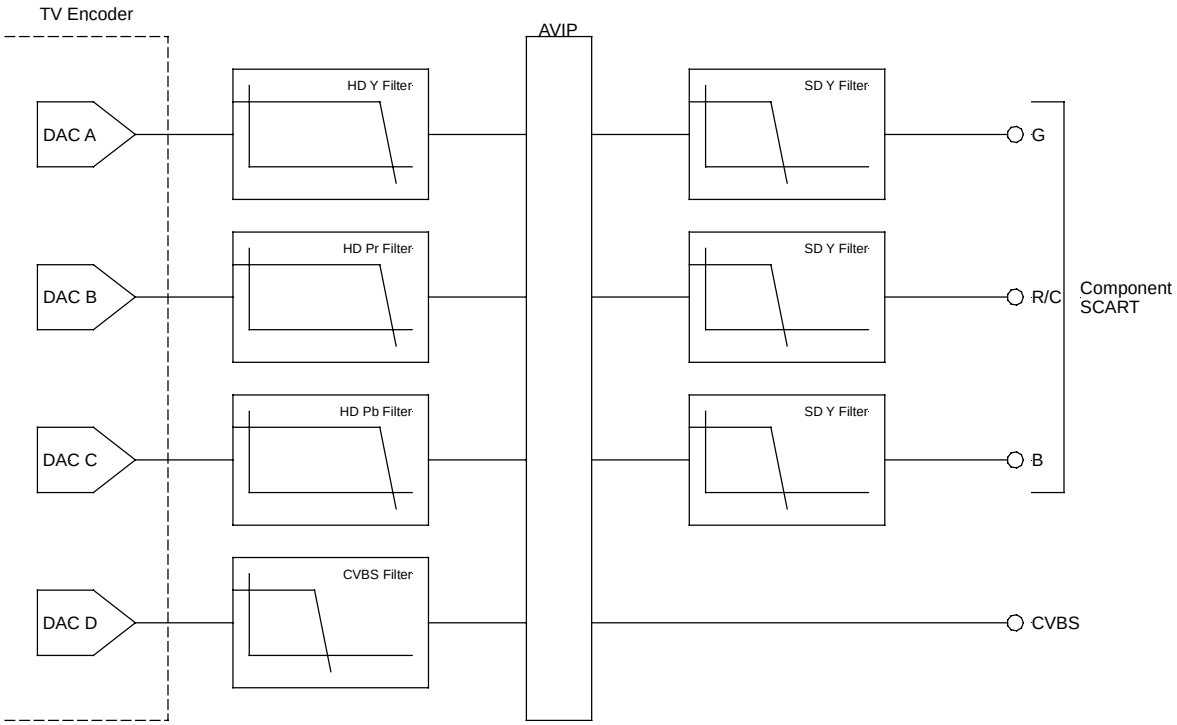


Figure 45. Video Filter Arrangement, Component SCART Mode

2.12.6.3. HDTV Mode

In HDTV, the TV Encoder outputs analog Luminance (Y) and two color difference signals (Pr and Pb) as defined in EIA-770.3. The fourth video output (dedicated to CVBS in SDTV mode) is not used in HDTV mode.

The Xbox OS can select any of the supported ATSC resolutions when the HDTV AV Pack is connected to the Xbox.

The figure below shows the filter arrangement for HDTV mode:

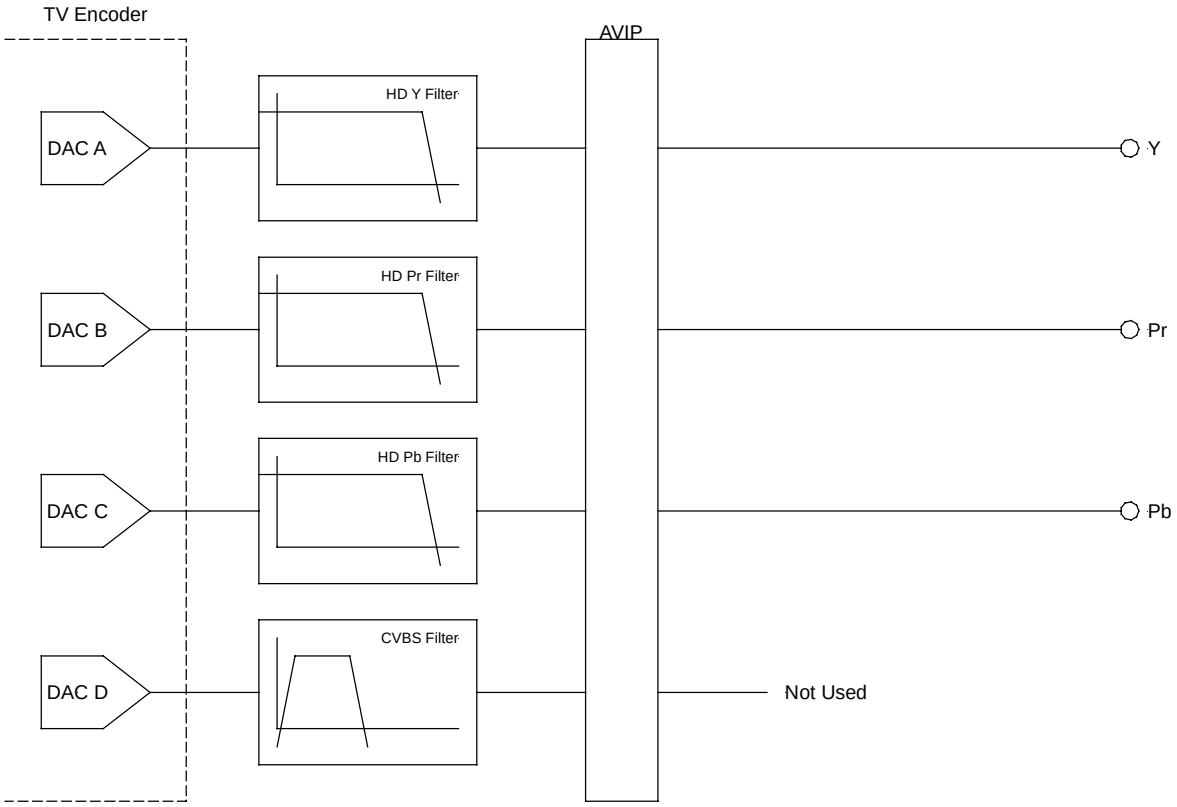


Figure 46. Video Filter Arrangement, HDTV Mode

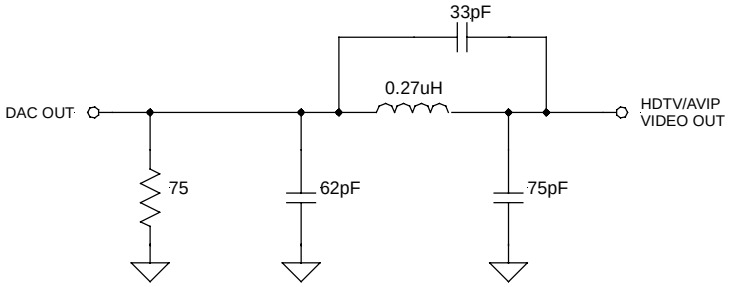


Figure 47. HDTV Filter Circuit

Parameter	Min	Typical	Max	Unit
HDTV Y Filter				
F_{LO} (-3dB)	0			MHz
F_{HI} (-3dB)			80	MHz
Attenuation @ 80MHz	60			dB
HDTV Pr/Pb Filter				
F_{LO} (-3dB)	0			MHz
F_{HI} (-3dB)			80	MHz
Attenuation @ 80MHz	60			dB

Figure 48. Analog Video Filter Architecture, HDTV Mode

2.12.6.4. VGA Mode

The AVIP supports a VGA mode interface for development purposes only. Compatibility with all VESA monitors is not guaranteed. This section describes the VGA implementation for reference only.

The VGA Mode of the AVIP provides component RGB video signals and H and V sync signals only. The Xbox implementation of VGA does not provide DDC serial communication for monitor configuration. Electrically, the AVIP utilizes the RGB outputs as described in the Enhanced SCART mode section, with the addition of the horizontal and vertical SYNC signals as shown in the figure below:

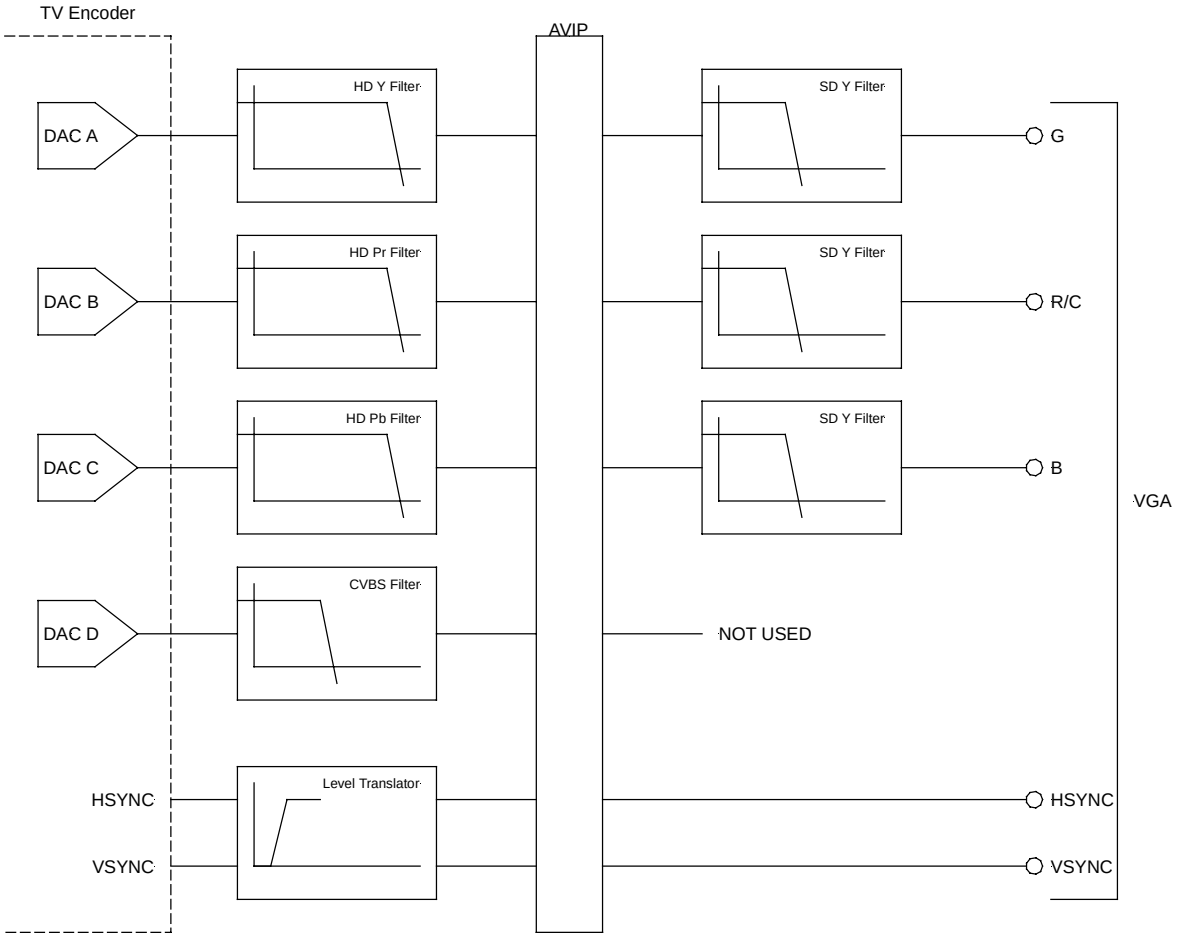


Figure 49. Video Filter Arrangement, Component SCART Mode

Refer to the Enhanced SCART Mode for filter characteristics. The level translator shown for HSYNC and VSYNC signals is provided to protect the TV Encoder and GPU from ESD, and to provide logic level translation from the low-voltage interface to TTL signaling levels required for VGA.

2.12.7. SCART Status Output

The AVIP port provides an output used to drive the SCART FUNCTION SWITCHING (pin 8 of the 21-pin Type II connector). The output levels expected at this pin are defined in EN-50049-1 as follows:

Parameter	Min	Typical	Max	Unit
Level 0 (Internal television broadcast reproduction)	0.0		2.0	V
Level 1A (Reproduction of source with 16:9 aspect ratio)	4.5		7.0	V
Level 1B (Peritelevision reproduction)	9.5		12	V
Output Resistance	300		1000	Ω
Rise time from Level 0 to Level 1B C_{LOAD} = 2nF, R_{LOAD} = 10kΩ			5	ms

Figure 50. SCART Aspect Ratio Control Signal Specifications

2.12.7.1. Functional Requirements

- Output characteristics shall be as defined in the previous table
- The output shall default to the Level 0 output level when power is off, or AC mains are disconnected. When Level 0 is asserted, the monitor device ignores the input video signals. If the monitor device is a television, it will automatically select its internal tuner as a video source.
- The Xbox shall programmatically select to output either the Level 0 or Level 1A, or Level 1B output conditions.
- Output Level 1B shall be asserted when the Xbox is outputting video in 4:3 aspect ratio.
- Output Level 1A shall be asserted when the Xbox is outputting video in 16:9 aspect ratio.

2.12.7.2. Electrical Implementation

The STATUS output is controlled by the state of two GPIO lines driven digitally to one of three legal states. The three legal states correspond to Level 0, Level 1A, and Level 1B according to the states of the control inputs. The control inputs are driven at 3.3V levels, according to the following table:

LVLCNT0	LVLCNT1	STATUS
LO	LO	Level 1B
HI	LO	Level 1A
HI	HI	Level 0
LO	HI	Undefined

Figure 51. Status Control State Diagram

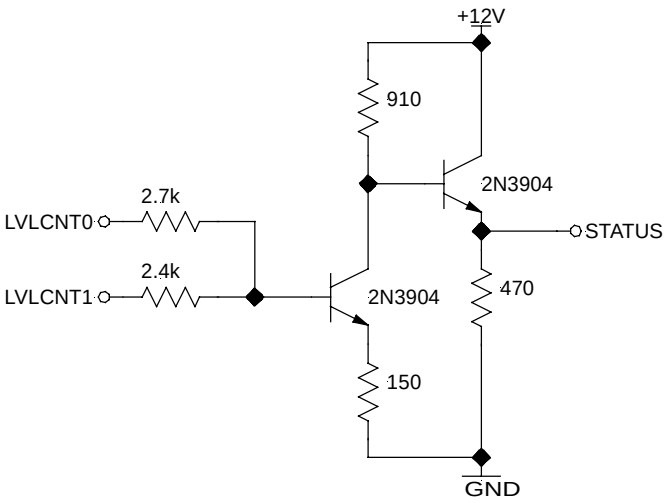


Figure 52. SCART Status Output Circuit

2.13. Controller Interface Port

The controller interface port provides a means of connecting peripheral devices to the Xbox. The port is designed primarily for game controller type devices, but may also be used for any other peripherals that are to be connected to the Xbox.

The port provides DC power, a bi-directional digital communication bus, and a video synchronization signal to support peripherals that utilize CRT timing (such as light guns). Each aspect of the controller port is discussed in the following sections.

2.13.1. Mechanical Specification

The mechanical connector used for the controller interface is a custom design for Xbox, but is based on the electrical specification of the Type A USB connector specified in the Universal Serial Bus Specification, Version 1.1. A fifth conductor is added to output the video sync signal.

Al though the electrical specification is based on USB Type A connector, the mechanical design is very different. The Xbox controller port connector is designed to be more robust in terms of insertion cycles, extraction force, and side pull durability.

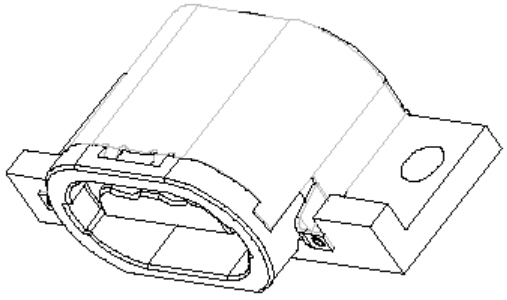


Figure 53. Controller Port Mechanical Sketch

Electromechanical Properties				
Parameter	**Min**	**Typical**	**Max**	**Unit**
Insertion Force			15	N
Withdrawal Force	10			N
Contact Retention Force (in housing)	1			N
Durability		5000		cycles
Contact Voltage (30 sec @ sea level)			250	VAC
Current, per contact			1.0	A
Insulation Resistance	500			MΩ
Dielectric Withstand Voltage (30 sec @ sea level)			500	VAC
Contact Resistance			30	mΩ
Contact Capacitance			2	pF

Material Specification	
Dielectric Material	Glass filled polybututylene terephthalate (PBT) or polyethylene terephthalate (PET) or equivalent
Contact Material	Phosphor Bronze or other high strength Copper alloy
Shell Material	Brass or other copper-based high-strength material 100µin Sn or SnPb over 50µin Ni
Contact Finish	30µin Au over 50µin Ni or 3µin Au Flash over 30µin PdNi over 50µin Ni

Pin	Signal Name	Direction	Comment
1	V_{BUS}	POWER	5V @ 500mA max Peripheral Power
2	D-	IO	USB V1.1 Differential Signaling Pair
3	D+	IO	
4	CSYNC	OUT	Composite Sync Output
5	GND	POWER	DC and signal return

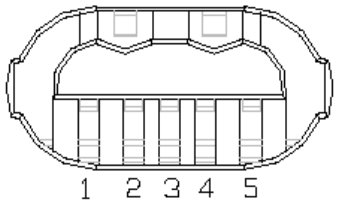


Figure 54. Controller Port Pin Out

2.13.2. DC Power Output

The controller port provides 5V bus power for powering the down stream peripherals, and incorporates overcurrent and undervoltage protection. The overcurrent protection circuits for the controller ports shall be designed to accommodate the inrush current requirements of a peripheral with loading characteristics as shown in the table.

Parameter	Min	Typical	Max	Unit
DC Output Voltage (V_{BUS}) No Load Max Load	 4.75	5.00	 5.25	V
DC Output Current, continuous			500	mA
Overcurrent Trip Point		750	1250	mA
Capacitive Loading (On Controller side of connector)			240	µF
Bulk Capacitance (On Console side of connector)		22		µF

Figure 55. Controller Port DC Power Specification

Over current protection is implemented by power management switches. IMP Part number IMP2524-1BWM (or equivalent) is specified. The ENABLE lines of this switch are active HIGH and are connected to GPIO pins on the MCPX as noted in the MCPX GPIO pin map. The overcurrent flag outputs are connected to pins on the MCPX dedicated to overcurrent flag input.

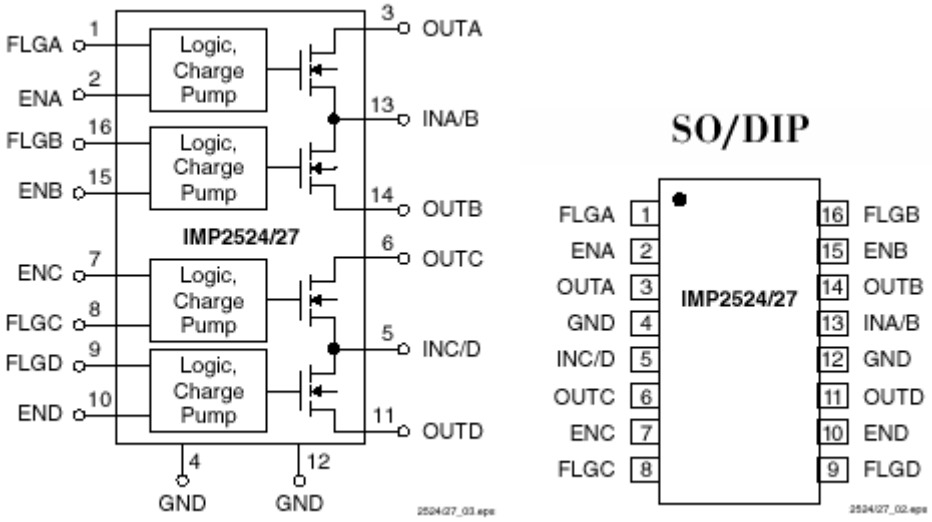


Figure 56. IMP2524 Power Management Switch

Provision is made on the motherboard for a fifth controller port. This port is populated for development units only, and provides an additional means of connecting debug equipment for test and development of software. The electronics and connector associated with this port are not populated in the production version of the Xbox. The following section describes the overcurrent protection of for the fifth port.

A single power management switch provides overcurrent protection of the fifth port. This switch is similar to that described above for the four main ports. The part number of this switch is IMP2525A-1BM. The pin out of this component is shown below:

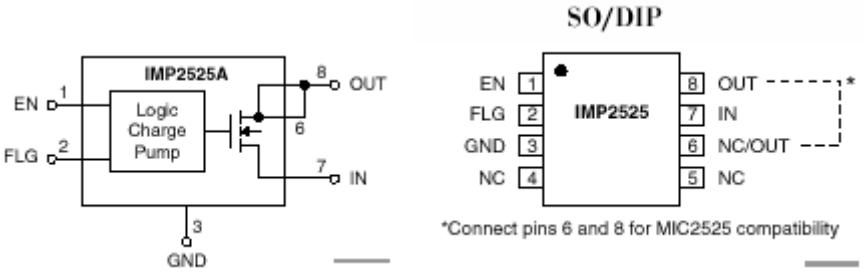


Figure 57. IMP2525A Power Management Switch

2.13.3. Digital Communication

The data interface is differentially signaled as per USB v1.1 specification, but only supports the Full Speed (12Mbits/sec) signaling protocol. The driver in XOS does not support all the USB class devices, thus this port is not truly a USB v1.1 port; it only utilizes the full-speed USB physical layer protocol.

The MCPX provides the differential transceivers connected to the four main controller ports.

The Xbox motherboard design supports a fifth controller port for development purposes only. This port is also driven by the MCPX, but the port is not populated in production units of Xbox.

2.13.4. Video Sync Signal

The NV2A GPU outputs a composite sync signal that is output to each of the controller ports. This signal is provided to support the implementation of controllers that need to have a timing reference to the CRT output. A light gun, that provides X,Y pointing input to the Xbox based on the location of the screen that it is pointed to is an example of such a controller.

Parameter	Min	Typical	Max	Unit
Voltage Output V_{OH} @ I_{OUT}=3mA V_{OL} @ I_{OUT}=5mA	2.8		 0.6	V
Output Impedance	33		300	Ω
Load Capacitance (C_{LOAD})			300	pF
Load Resistance (R_{LOAD})	5			kΩ
Slew Rate @ MAX C_{LOAD} and MIN R_{LOAD}		15		V/µS

Figure 58. CSYNC Signal Output Characteristics

Note:

The sync waveform is TBD pending implementation in the NV2A logic. The signal may or may not resemble a standard composite sync waveform, however, a down stream device shall be capable of determining both vertical and horizontal timing based on this signal.

2.14. LPC Header

The motherboard terminates the LPC interface in a standard debug LPC Header connector as described in the *Installable LPC Debug Module Design Guide*. This port is located on the motherboard and is not accessible from outside the chassis.

The debug LPC interface specified in the *Design Guide* includes several signal groups. These groups are listed below and exceptions from the controlling document are noted.

- PCI Reset – This signal is defined as an input to the Host and to the Peripheral in the referenced document, but in the Xbox it is an output driven from the MCPX, and is intended to reset the peripheral devices connected to the LPC.
- LPC Interface – This is the standard LPC signal group
- DC Power – The interface provides both 3.3 and 5 VDC power supplies. Overcurrent protection is not provided on the motherboard.
- SMBus Signals – SCL and SCK signals from the primary SMBus are connected to the SMBus pins on the debug header. Refer to the SM Bus map in Appendix C for further details.
- EEPROM strapping resistors – These pins are generally provided for address strapping options to the peripheral device. These pins are left unterminated in the Xbox implementation.

2.14.1. Mechanical Specification

The header is a 100-mil pitch dual-row square-pin header as shown in the figure below. Note that the document describes both a 16-pin and 20-pin interface, the Xbox implements the 16-pin option. Pin 4 is voided in the header to provide positive keying with the cable receptacle.

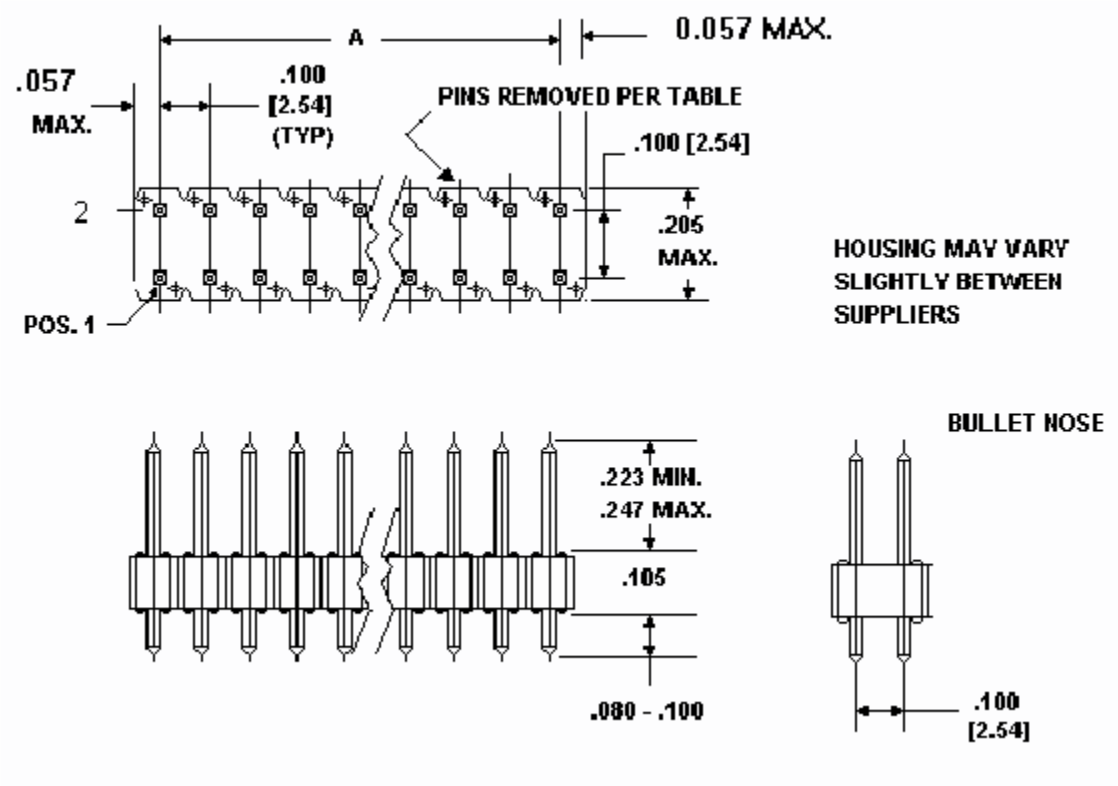


Figure 59. LPC Interface Header (Dimension A=0.70 inches)

2.14.2. Signal List

Pin	Signal Name	Direction	Comment
1	LCLK	OUT	This is a 3.3 VDC PCI clock. This clock must meet PCI signal requirements including maximum skew with respect to the other PCI clocks in the system.
2	VSS	POWER	System Ground
3	LFRAME#	OUT	This signal is used to indicate the start and termination of cycles on the LPC interface. This is a 3.3 VDC signal.
4			This pin voided in header to ensure correct alignment of the cable receptacle.
5	LRST#	OUT	PCI reset signal driven by the MCPX
6	VCC5		5VDC power supply
7	LAD3#	I/O	Multiplexed Command, Address, and Data
8	LAD2#	I/O	Multiplexed Command, Address, and Data
9	VCC3	POWER	3.3VDC Power Supply
10	LAD1#	I/O	Multiplexed Command, Address, and Data
11	LAD0#	I/O	Multiplexed Command, Address, and Data
12	VSS	POWER	System Ground
13	SCL	I/O	SMBus clock signal
14	SDA	I/O	SMBus data signal
15	SPDA1	-	This is pin generally is the hardware address input A1 on the serial EEPROM device on the module. This pin is left unterminated in the Xbox implementation.
16	SPDA0	-	This is pin generally is the hardware address input A0 on the serial EEPROM device on the module. This pin is left unterminated in the Xbox implementation.

Figure 60. LPC Header Pin Out

2.15. Power Supply

This section describes the assumptions and design guidelines related to the Xbox power supply. The power supply is implemented as three functional blocks. A system Power Supply Unit (PSU) provides the bulk power conversion from the AC line input to regulated DC voltages. Local regulation on the motherboard converts the PSU outputs for the critical core voltage supplies required by the CPU, GPU, and DDR memory. Other local regulators provide low-noise analog power supplies for the audio and video sections. Lastly, a battery powered supply provides power to maintain the real time clock and NVRAM contents when line power is unavailable.

The power supply shutdown is controlled by the System Management Controller, as described in the section of this document devoted to the SMC. The system PSU must provide a low-current supply voltage to the SMC at all times, this output is referred to as **3VSB** in the block diagram. This supply is active at all times, as long as the supply is connected to the AC mains to provide power for the SMC and to charge the RTC/NVRAM backup battery.

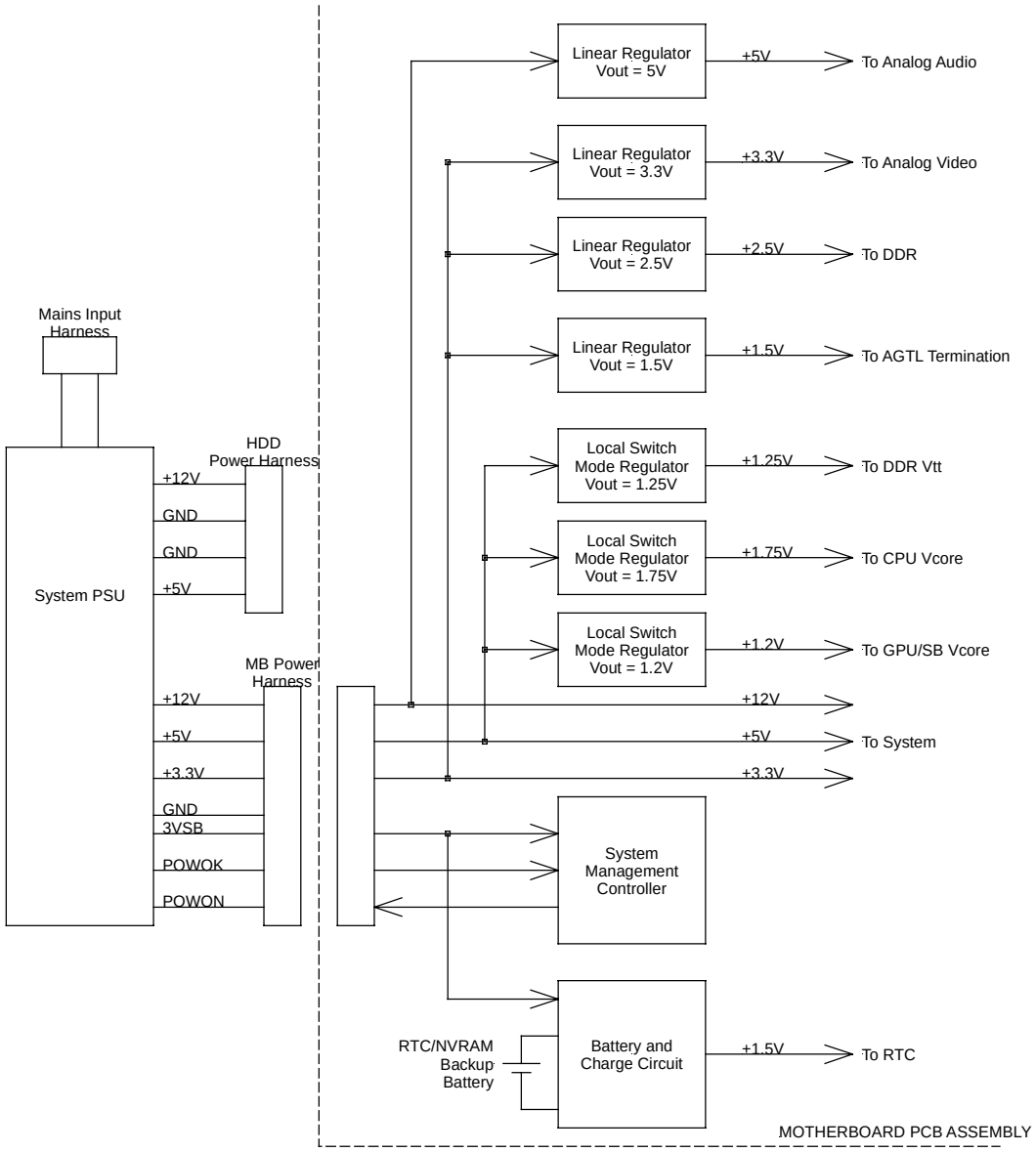


Figure 61. Power Supply Block Diagram

2.15.1. System Power Budget

The Power budget for Xbox is based on both peak and average power consumption of each of the major functional blocks of the system. The system PSU provides bulk power that is locally regulated for the CPU, GPU, core logic, memory, and analog systems. A detailed power budget spread sheet can be found in Appendix A.

2.15.2. System PSU

The System PSU is described in detail in Power Supply Design Spec.doc with the key functional specifications are summarized in the tables below.

PSU Input Specifications				
Parameter	**Min**	**Typical**	**Max**	**Unit**
Input Voltage Low Range High Range	 88 180	 110 230	 135 265	VAC
Input Frequency	47		63	Hz
Input Current Low Range High Range			 2.4 1.2	A_{RMS}
Internal Fuse current limit			TBD	A_{RMS}
Inrush Current			TBD	A

PSU System Specifications				
Parameter	**Min**	**Typical**	**Max**	**Unit**
Total Power Output Continuous (@ Typical loading of all outputs) Peak (duration less than 10 sec)		96	 160	W
Efficiency, at typical load on each output	80			%
PSU Heat Dissipation (at typical output loading at minimum efficiency)			24	W
Holdup Time (at nominal input voltage and typical output loading)	17			ms
Power Factor (European and Japanese configurations only)	TBD			%

PSU Disk Drive Output Specifications					
Parameter		**Min**	**Typical**	**Max**	**Unit**
12V Output (±5% @ Typical Current) (+5/-8% @ Peak Current)	Output Voltage At typical load current At peak load current	 11.40 11.04	12.00	12.60	V
	Output Current	0.0	0.6	2.9	A
5V Output (+5%/-4%)	Output Voltage	4.80	5.00	5.25	V
	Output Current	0.0	0.5	1.5	A

PSU System Power Output Specifications					
Parameter		**Min**	**Typical**	**Max**	**Unit**
12V Output (±5% @ Typical Current) (+5/-8% @ Peak Current)	Output Voltage At typical load current At peak load current	 11.40 11.04	12.00	12.60	V
	Output Current	0.05	0.6	2.1	A
5V Output (+5%/-4%)	Output Voltage	4.80	5.00	5.25	V
	Output Current	2.5	12.7	17.5	A
3.3V Output (±5%)	Output Voltage	3.14	3.30	3.47	V
	Output Current	1	4.8	6.5	A
3VSB Output (±5%)	Output Voltage	3.14	3.30	3.47	V
	Output Current	0	20	50	mA

2.15.3. RTC Power Supply

The Real Time Clock is maintained on time when the power is off and the unit is unplugged by means of a secondary battery. The battery is charged whenever the unit is plugged into the AC power mains, regardless of whether the user turns “ON” the unit. This is accomplished by using a rechargeable battery that is kept charged by the 3VSB power supply, which also powers the system microcontroller.

Parameter	Specification
Battery Chemistry	Manganese Titanium Lithium (MnTiLi)
Type	Panasonic MT Series (MT920)
Nominal Voltage	1.5V
Capacity	5mAh

The cell is charged from the standby power supply, and thus the RTC does not drain power from the cell unless mains power is removed from the unit. The recharge circuit is a constant-voltage type, with a low-current shunt regulator to protect the RTC supply pins from over voltage.

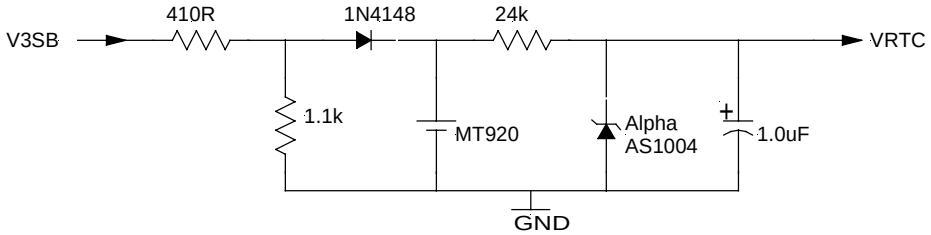


Figure 62. RTC Battery Charge Circuit

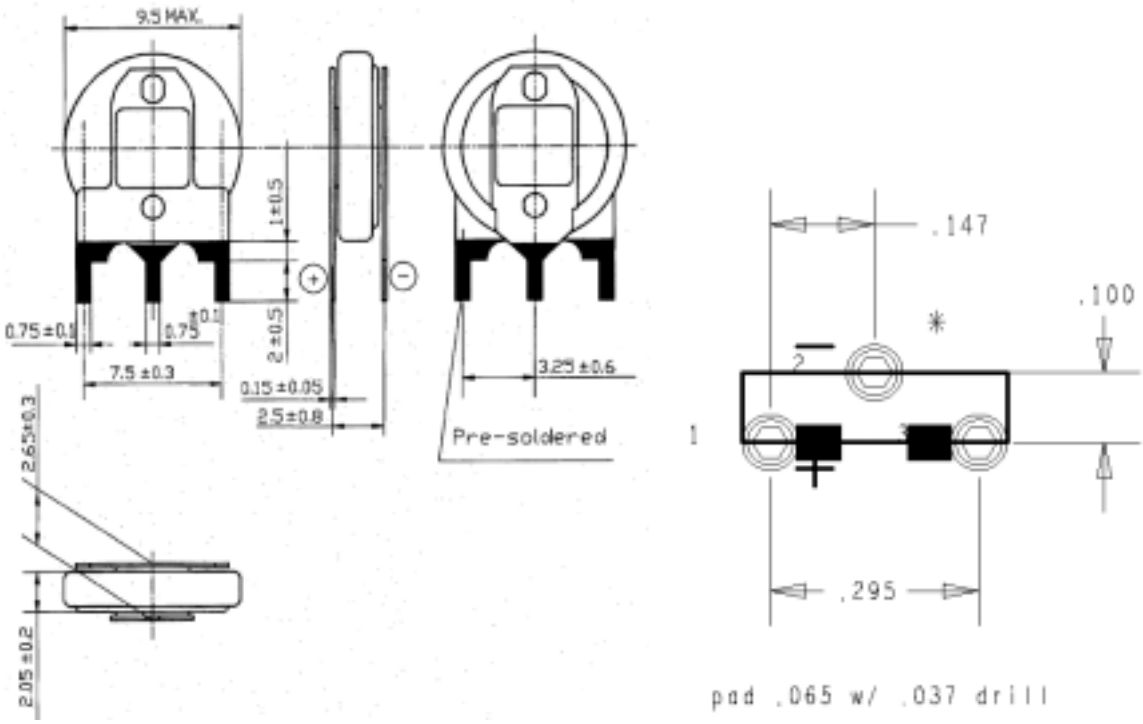


Figure 63. MT-920 Battery Footprint

Note:
The footprint shown in the figure above is tentative only, however it is expected to be very close to the final design. The final footprint is pending review from Flextronics and Panasonic. The EVT design shall use a socket footprint for a bare MT-920 cell, the final footprint shall be incorporated into the DVT design.

2.15.4. Local Voltage Regulators

The motherboard implements both switch-mode and linear voltage regulators to provide spot regulation of critical voltages. The input and output specifications for each of these regulator circuits are specified below:

Note:

Completion of the following tables is pending input from Intel.

2.15.4.1. Switch-Mode Voltage Regulators

Parameter		Min	Typical	Max	Unit
GPU/SB V_{CORE}	Voltage Input		5		V
	Voltage Output	1.45	1.50	1.55	V
	Current Output	TBD	7.0	9.8	A
	Transient				
	Temp Coeffcient				
	Efficiency		80		%
	Heat Dissipation		2.1		W
CPU V_{CORE}	Voltage Input		5		V
	Voltage Output	TBD	1.75	TBD	V
	Current Output		18.6	20.5	A
	Efficiency		80		%
	Heat Dissipation		8.1		W
DDR V_{TT}	Voltage Input		5		V
	Voltage Output	TBD	1.25	TBD	V
	Current Output		5.0	5.5	A
	Efficiency		80		%
	Heat Dissipation		6.5		W

2.15.4.2. Linear Regulators

Parameter		Min	Typical	Max	Unit
CPU V_{TT}	Voltage Input		3.3		V
	Voltage Output	TBD	1.5	TBD	V
	Current Output		0.8	1.7	A
	Heat Dissipation		1.5		W
DDR V_{CORE}	Voltage Input		3.3		V
	Voltage Output	TBD	2.5	TBD	V
	Current Output		3.9	4.3	A
	Heat Dissipation		3.1		W
Analog 3.3V (Video)	Voltage Input		5		V
	Voltage Output	3.14	3.3	3.47	V
	Current Output		200	300	mA
	Heat Dissipation		340		mW
Analog 5V (Audio)	Voltage Input		12		V
	Voltage Output	4.75	5.00	5.25	V
	Current Output		300	400	mA
	Heat Dissipation		2.1		W

3. Xbox Accessories

3.1. Game Controller

The game controller interfaces to the Xbox via the Xbox Controller Port described in section 2.13. The Xbox Game Controller is described in detail in the *Xbox 3rd Party Game Controller Specification*. The Game Controller includes two module slots, each having a USB signaling pair associated with it. The controller includes an embedded hub device that logically breaks out the two downstream ports.

The USB interface to the Game Controller is based on USB v1.1, with exceptions as listed in the following paragraphs:

3.1.1.1. Xbox Exceptions to the Full Speed USB 1.1 Specification

- No low speed device USB support
- No suspend/resume support

3.1.1.2. USB Device Function

- Proprietary XID class device, as described in the *Xbox Game Controller Firmware Specification*
- 1 control end point
- 1 interrupt in endpoint
- 1 interrupt out endpoint

3.1.1.3. USB Hub Function

- 1 control end point (end point 0)
- downstream port 1: internally attached to game pad function
- downstream port 2: primary module slot
- downstream port 3: secondary module slot

3.1.1.4. USB Enumeration of Downstream Slots

- For top/bottom orientation: the top slot is primary, bottom slot secondary
- If module slots have left right orientation: (while holding the controller) left is primary, right is secondary

3.2. AV Packs

The Xbox is connected to television and audio equipment by use of intermediate cable sets referred to as AV Packs. The AV Packs break out the video and audio signals to connectors suited to interface to various types of AV equipment. In addition to providing connector adaptation, the AV Packs provides information to the Xbox that enables the Xbox to tailor the output signals as necessary.

For example, if the Standard NTSC AV pack is connected, the Xbox automatically configures its output for composite NTSC output and stereo analog audio output. If the NTSC RFU AV pack is connected, the Xbox configures its output for NTSC composite and s-Video, and mono audio output.

The AV Packs are described in detail in the Xbox AV Pack Design Specification.doc. The contents of this document are summarized below:

3.2.1.1. Standard NTSC A/V Pack

The Standard AV Pack connects to the Xbox AV interface port and provides Composite Video Out, and line-level stereo audio out. The video and audio outputs are output on standard consumer video phono-type plugs.

Composite Video Out – One consumer video phono type cable connector. The cable must be shielded, nominal impedance of 75Ω, and the shield shall provide a minimum of 85% coverage, such as UL Type 1354 (26 or 28 AWG) or equivalent.

Analog Audio Out (Left) – One consumer audio phono-type connector. Cable shall be shielded (spiral or braided), such as UL type 1185 (26 AWG) or equivalent.

Analog Audio Out (Right) – One consumer audio phono-type connector. Cable shall be shielded (spiral or braided), such as UL type 1185 (26 AWG) or equivalent.

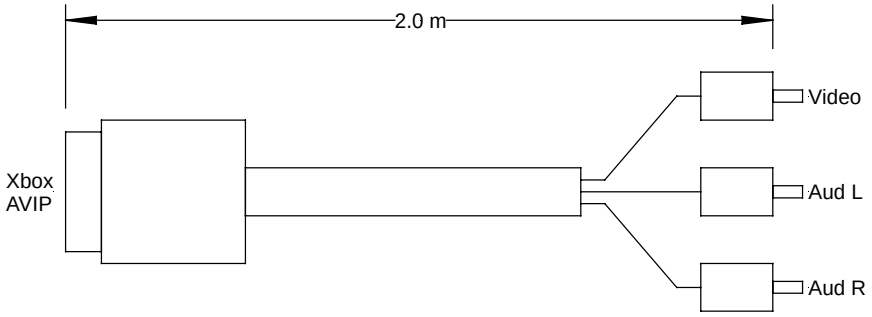


Figure 64. Standard A/V Pack

3.2.1.2. Standard PAL AV Pack

The Standard AV Pack connects to the Xbox AV interface port and provides Composite Video Out, and line-level stereo audio out. The video and audio outputs are output on standard consumer video phono-type plugs.

Composite Video Out – One consumer video phono type cable connector. The cable must be shielded, nominal impedance of 75Ω, and the shield shall provide a minimum of 85% coverage, such as UL Type 1354 (26 or 28 AWG) or equivalent.

Analog Audio Out (Left) – One consumer audio phono-type connector. Cable shall be shielded (spiral or braided), such as UL type 1185 (26 AWG) or equivalent.

Analog Audio Out (Right) – One consumer audio phono-type connector. Cable shall be shielded (spiral or braided), such as UL type 1185 (26 AWG) or equivalent.

The layout of the Standard PAL AV Pack is identical to that of the Standard NTSC AV Pack. Note that the two differ only in the MODE jumpers that identify the pack to the Xbox.

3.2.1.3. SCART Adapter

The SCART Adapter is used to adapt the Standard PAL AV Pack to televisions equipped with a SCART style connector. In this configuration, the SCART interface provides only Composite video output and stereo audio.

The Adapter consists of a SCART connector and three phono-style input jacks for composite video, left audio, and right audio as output from the Standard PAL AV Pack.

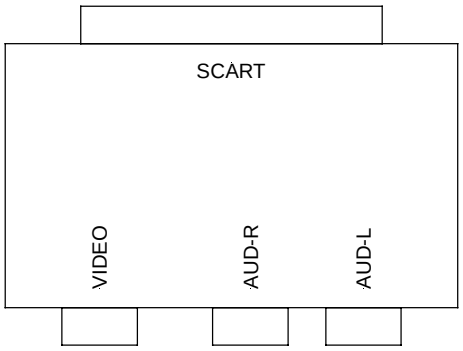


Figure 65. SCART Adapter

3.2.1.4. Standard SCART AV Pack

The Standard SCART AV Pack for the European market provides a means of attaching the Xbox to a television monitor with SCART input. The Xbox SCART connector conforms to the electrical interface and impedances described in EN 50049-1, and is upwardly compatible with the chain interconnection system described in EN 50157-2-1. The Xbox SCART plug is designed to plug into a Type I SCART port on a television monitor or other audio/video equipment.

The Standard SCART AV Pack only supports the PAL TV Mode, and provides composite video as the only video signal option. s-Video and RGB component modes are not supported by this AV Pack..

Type II SCART Plug– One 21-pin plug conforming to EN 50049-1. This connector carries linear left and right audio and composite or s-video, as selected under software control.

Internal Jumper Wires – The mode input pins are internally jumped using solid jumper wire, 30AWG or larger, as indicated in the schematic diagram.

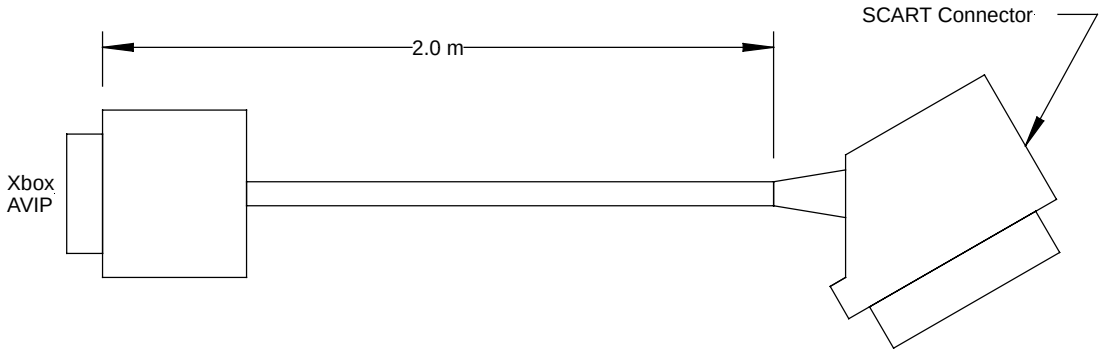


Figure 66. Standard SCART AV Pack Mechanical Layout

Note:

This AV Pack may be dropped from the final list of AV Pack variations pending marketing input.

3.2.1.5. Enhanced NTSC A/V Pack

The Enhanced NTSC AV Pack connects to the Xbox AV interface port and provides suitable for low-end consumer home theater, including s-Video output and optical SP-DIF output for digital sound. The Enhanced AV Pack retains the composite video and linear audio outputs as well to accommodate various system configurations.

Additionally, the Enhanced NTSC A/V pack supports the use of headphones for private listening. Note- when headphones are used, the line and SP/DIF outputs are not muted.

The outputs of the Enhanced NTSC AV pack are listed below:

Composite Video Out – One consumer video phono type jack.

Analog Audio Out (Left) – One consumer audio phono type jack.

Analog Audio Out (Right) – One consumer audio phono type jack.

S-Video Out – One DIN-4 consumer s-Video output Jack.

SP-DIF Digital Audio Output – One jack for optical output of SP-DIF digital audio out. The connector shall comply with EIAJ CP-1201.

Headphone Out – One 3.5mm stereo jack for connecting a pair of 20Ω headphones.

Volume Control – Two momentary type push buttons to increase and decrease volume levels.

The Enhanced NTSC AV Pack is constructed using “lump on a line” construction, in that the Xbox AVIP connector terminates to a cable assembly, which in turn terminates into a breakout box containing the AV connectors listed above.

The cable assembly connecting the AVIP plug to the breakout box consists of an over-molded assembly of individual conductors. The composite and s-Video signals (V, Y, and C) are carried on coaxial cable with 75Ω characteristic impedance (UL 1354 or equivalent). The left and right audio signals are carried on spiral-shielded cable (UL 1185 or equivalent). The remaining conductors are stranded wire, 26AWG (UL type 1007? or equivalent).

The mechanical layout and schematic of the Enhanced AV PACK are shown below:

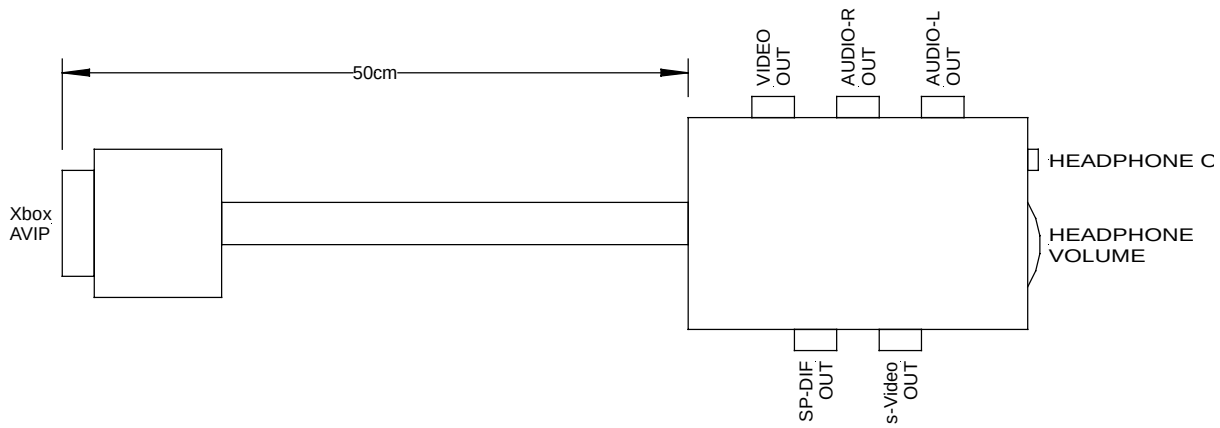


Figure 67. Enhanced NTSC A/V Pack Mechanical Layout

3.2.1.6. Enhanced SCART AV Pack

The Enhanced SCART AV Pack for the European market provides a means of attaching the Xbox to television monitor with SCART input. The Xbox SCART connector conforms to the electrical interface and impedances described in EN 50049-1, and is upwardly compatible with the chain interconnection system described in EN 50157-2-1. The Xbox SCART plug is designed to plug into a Type I SCART port on a television monitor or other audio/video equipment.

The Enhanced SCART connector outputs stereo audio and video, which may be selected from one of three modes; composite video, s-video, or RGB. Upstream aspect ratio is controlled by outputting one of three voltages on the STATUS/ASPECT RATIO pin of the SCART connector as specified in EN50049-1.

In addition to the 21-pin SCART connector, the Enhanced SCART AV Pack also provides an optical SP-DIF connector for digital audio and a headphone amplifier as described in the Enhanced NTSC AV Pack.

Type II SCART Plug– One 21-pin plug conforming to EN 50049-1. This connector carries linear left and right audio and s-video.

SP-DIF Digital Audio Output – One jack for optical output of SP-DIF digital audio out. The connector shall comply with EIAJ CP-1201.

Headphone Out – One 3.5mm stereo jack for connecting a pair of 20Ω headphones.

Volume Control – One rotary volume control for adjusting the headphone volume.

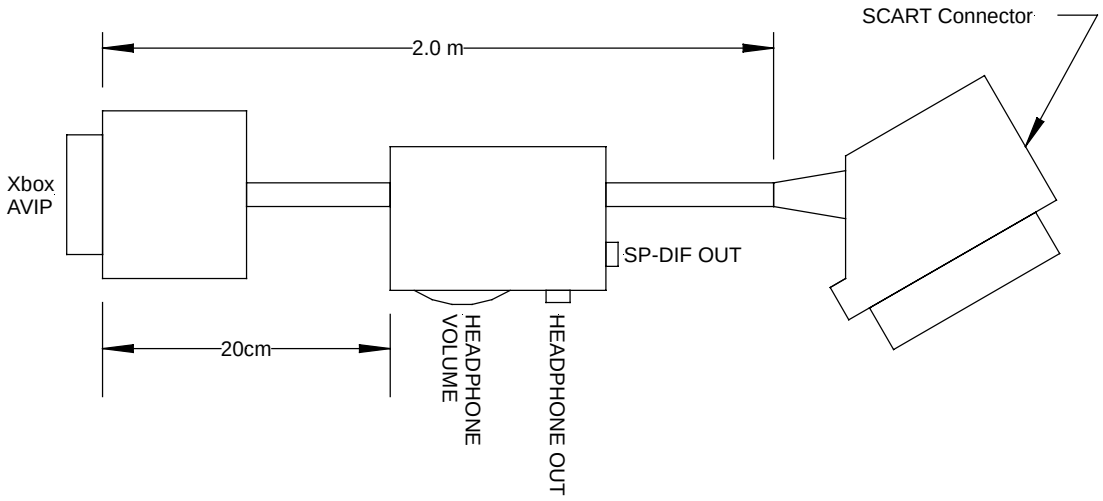


Figure 68. Enhanced SCART AV Pack Mechanical Layout

3.2.1.7. NTSC Video RF Unit AV Pack

The NTSC Video RFU is an AV Connector Pack that provides an RF modulated television signal for connection to an NTSC television ANT input. This is a localized module specific to the region in which the AV pack is sold; the NTSC countries are listed in the table included in this section.

The RFU module takes as inputs the composite video and mono audio signals from the AVIP connector and outputs a single RF modulated signal via an RF connector. The module must have a channel select switch that selects one of two channels to modulate on to.

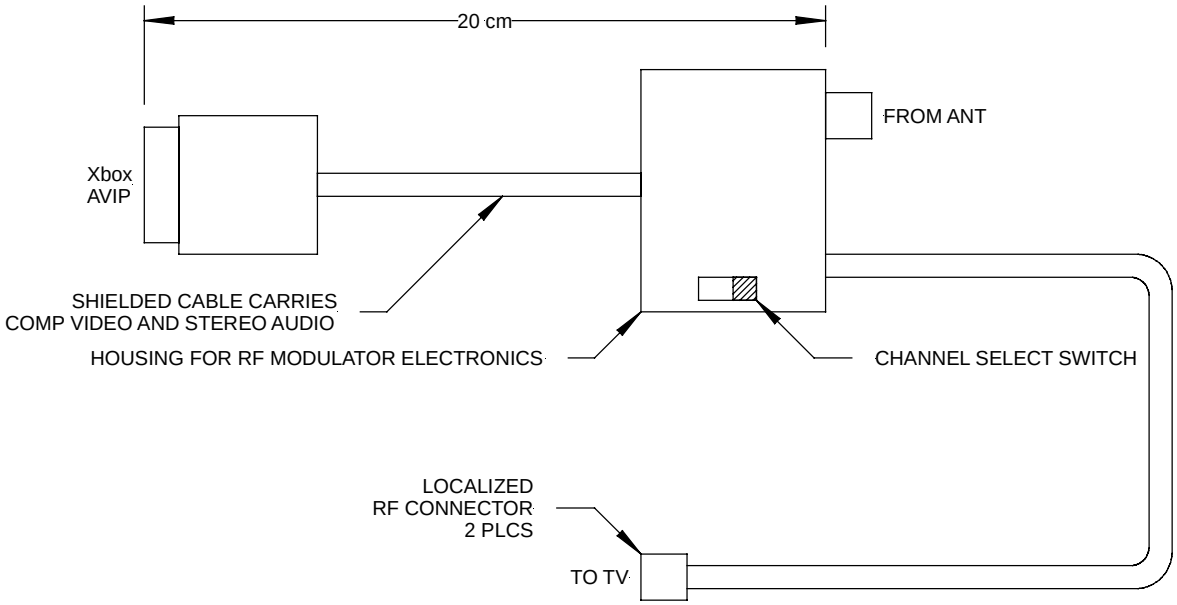


Figure 69. NTSC Video RFU AV Pack

Market	Television Format	Channels	Connector
USA	NTSC/M (525 lines 29.97f/s)	VHF 3 or 4 Selectable by switch	F-Type Coaxial
Canada	NTSC/M (525 lines 29.97f/s)	VHF 3 or 4 Selectable by switch	F-Type Coaxial
Mexico	NTSC/M (525 lines 29.97f/s)	VHF 3 or 4 Selectable by switch	F-Type Coaxial
Japan	NTSC (525 lines 29.97f/s)	VHF 3 or 4 Selectable by switch	F-Type Coaxial

Figure 70. NTSC Video RFU Localization

3.2.1.8. PAL Video RF Unit AV Pack

The PAL Video RFU is an AV Connector Pack that provides an RF modulated television signal for connection to a PAL television ANT input. This is a localized module specific to the region in which the A/V pack is sold. In Europe there are four modulation formats; PAL-I, PAL B/G, PAL-B/H, and SECAM-L. The table in this section shows the modulation format by country.

The RFU module takes as inputs the composite video and mono audio signals from the AVIP connector and outputs a single RF modulated signal via an RF connector. The module must have a channel select switch that selects one of two channels to modulate on to.

Refer to the figure in the previous section for the mechanical layout of the PAL RFU as it is identical to that of the NTSC RFU, with the only exception being the style of the RF connector. The electrical schematic is identical to the NTSC RFU except for the pin location of the jumper wire. A schematic for the PAL RFU is included in this section.

Market	Television Format	Channels	Connector
United Kingdom Ireland	PAL-I (625 lines 25f/s)	VHF 3 or 4 Selectable by switch	9.5mm Coaxial
France	SECAM-L (625 lines 25f/s)	VHF 3 or 4 Selectable by switch	9.5mm Coaxial
Germany Spain Italy Netherlands Norway Sweden Finland Austria New Zealand	PAL-B/G (625 lines 25f/s)	VHF 3 or 4 Selectable by switch	9.5mm Coaxial
Luxembourg	PAL-B/G SECAM-L (625 lines 25f/s)	VHF 3 or 4 Selectable by switch	9.5mm Coaxial
Belgium	PAL-B/H (625 lines 25f/s)	VHF 3 or 4 Selectable by switch	9.5mm Coaxial

Figure 71. Video RFU Localization

3.2.1.9. HDTV AV Pack

The HDTV AV Pack connects the Xbox to a High-Definition Television Monitor equipped with a component Y/Pr/Pb (or Y/U/V) interface as specified in EIA 770.3. The HDTV AV Pack provides consumer phono jacks for analog line level audio output. Digital audio output is provided by an optical SP-DIF jack.

HDTV Out – Three consumer phono style plugs for Luminance (Y) and two color difference signals (Pr and Pb) color coded green, red, and blue respectively.

Analog Audio Out (Left) – One consumer audio phono type jack.

Analog Audio Out (Right) – One consumer audio phono type jack.

SP-DIF Digital Audio Output – One jack for optical output of SP-DIF digital audio out. The connector shall comply with EIAJ CP-1201.

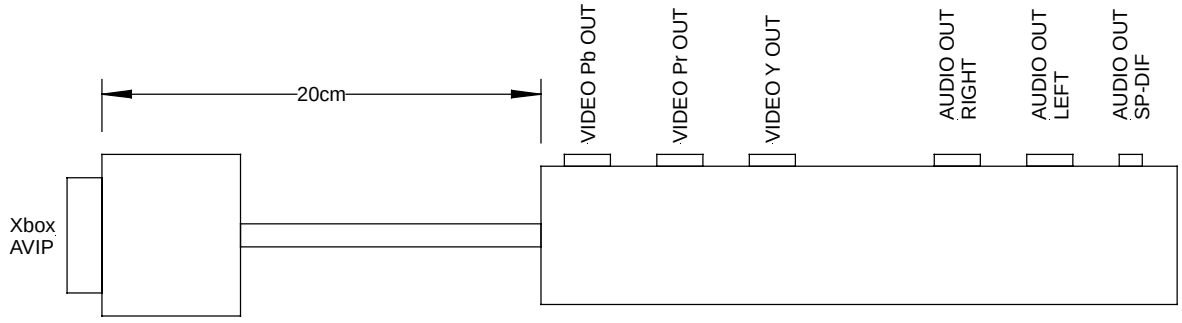


Figure 72. HDTV AV Pack Mechanical Layout

4. System Integration

This section describes the manner in which the Xbox console is broken down into electrical sub assemblies for manufacturability. This section describes only the electrical and electro-mechanical sub assemblies of the Xbox. Mechanical and cosmetic plastic components and sub assemblies are outside the scope of this section.

The block diagram below shows the top-level assembly block diagram and the manner in which the sub assemblies are interconnected:

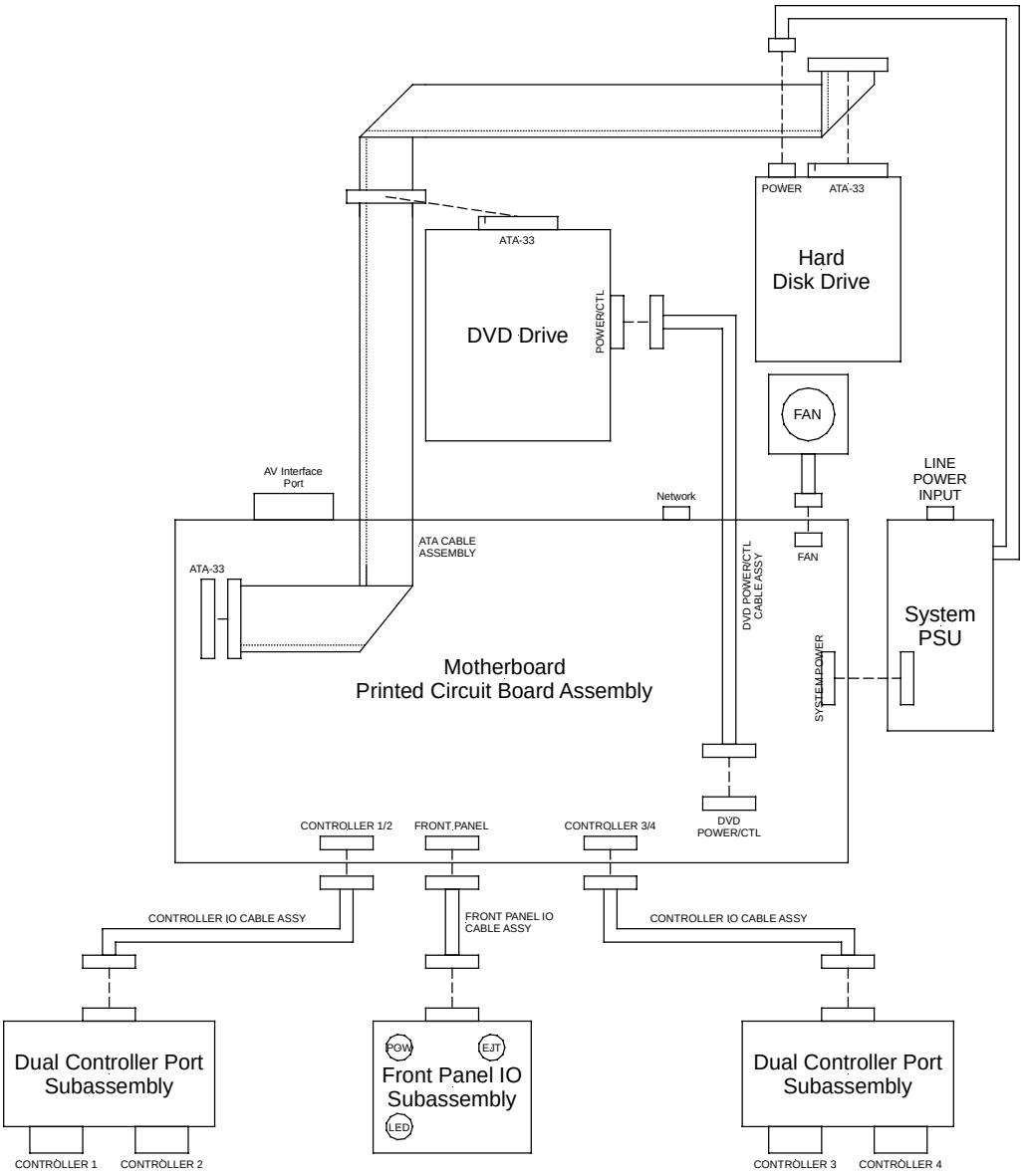


Figure 73. Xbox Top-Level Assembly Block Diagram

4.1. Motherboard Printed Circuit Board Assembly

The motherboard printed circuit assembly includes all the core logic, memory, physical interface and local power supply regulation described in this design specification. Rear-penal IO, including the Network, A/V interface, and Expansion port are directly mounted on the motherboard PCBA. Front panel IO and system power supply are implemented in subassemblies described later in this section.

The following subparagraphs describe the individual ports used to connect the motherboard to the other subassemblies.

4.1.1. System Power

This header mates directly to a matching receptacle on the system PSU. The header is Molex part number 42491-0322 or equivalent.

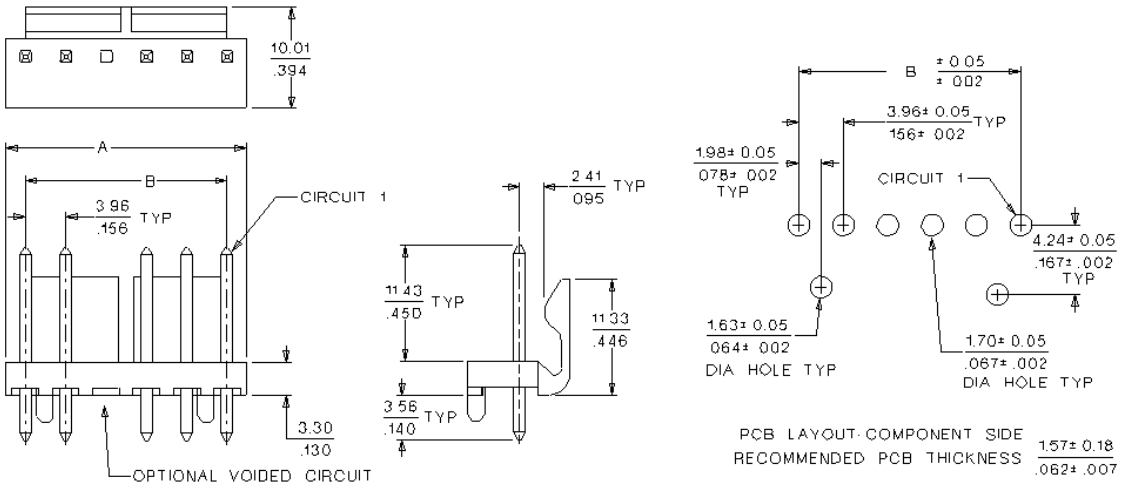


Figure 74. Motherboard Power Input Connector
A=47.40mm, B=43.59mm

This pin out for this connector is described in the figure below.

Pin	Signal Name	Direction	Comment
1	+12V	POW	+12 VDC Power Supply Output
2	+5V	POW	+5 VDC Power Supply Output
3	+5V	POW	+5 VDC Power Supply Output
4	+5V	POW	+5 VDC Power Supply Output
5	+3.3V	POW	+3.3 VDC Power Supply Output
6	+3VSB	POW	+3.3VDC Standby Power Supply Output
7	GND	POW	DC Return
8	GND	POW	DC Return
9	GND	POW	DC Return
10	GND	POW	DC Return
11	POWON	IN	Assert HIGH to enable +12V, +5V, and +3.3V outputs
12	POWOK	OUT	Asserted HIGH when all power supply outputs within specified levels

Figure 75. Motherboard System Power Header Pin Out

4.1.2. ATA

This connector conforms to the standard 40-pin AT-Attachment Connector specified in ANSI SFF-8059. The connector pin-out is described in section 2.8.3.1 Figure 14.

The header is keyed by removal of pin 20.

Header shroud shall be keyed.

Pin 28, reserved for cable select, shall be unterminated.

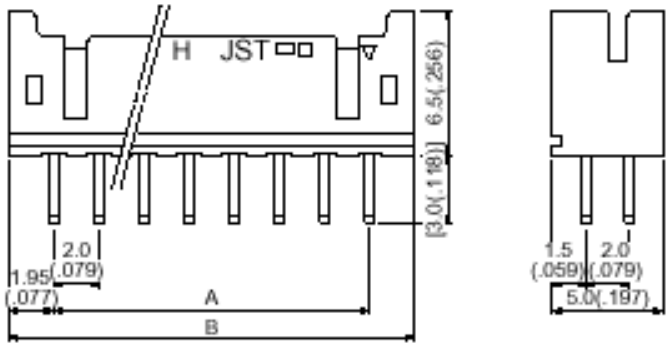
4.1.3. Controller 1/2 Port

This connector includes signals to support the physical interface to controller ports 1 and 2. The signals included on this connector, are as shown below:

Pin	Function	Pin	Function
1	VBUS1	2	1DM
3	DP1	4	SYNC1
5	GND1	6	SHLD
7	DM2	8	VBUS2
9	SYNC	10	DP2
11	KEY	12	GND2

Figure 76. Controller 1/2 Port Pin Out

The connector shall be JST Part Number B12B-PHDSS or B12B-PHDSS-B or equivalent. A sketch of the connector is shown below:



A=10.0mm, B=13.9mm

Figure 77. Controller 1/2 Port Connector

4.1.4. Controller 3/4 Port

This port is identical to the Controller 1/2 Port Connector described in the previous paragraph. The connector type and pin-out are identical, where Port 1 maps to Port 3 and Port 2 maps to Port 4.

4.1.5. Front Panel

This connector is used to interface the front panels controls (Power, Eject) and the front panel indicator LEDs to the motherboard logic. The signals included on this connector are shown in the table below:

Pin	Function	Pin	Function
1	GND	2	POWER SW
3	GND	4	EJECT SW
5	LED1 (Geen)	6	LED1 (Red)
7	LED2 (Red)	8	KEY
9	NO CONNECT	10	LED2 (Green)

Figure 78. Front Panel IO Connector Pin Out

Refer to the Front Panel IO section for a schematic of the signals on this connector.

4.1.6. DVD Power/Control

This connector provides control and status signals to and from the DVD drive controller.

The connector shall be JST Part Number B14B-PHDSS or B14B-PHDSS-B or equivalent. Refer to the figure below for a mechanical description of the connector. Note that dimensions A=12.0mm and B=15.9mm.

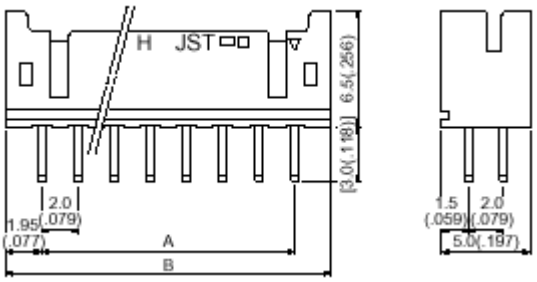


Figure 79. DVD Power/Control Jack on Motherboard

The pin out of this connector differs slightly from that of the connector on the DVD drive. Two additional pins are added on this connector in order to provide a method of keying the connector on the motherboard, preventing reverse-insertion during manufacturing. The pin out of this connector is shown below:

Pin	Signal Name	Direction	Comment
1	12VDC	POWER	12VDC for motor control
2	5VDC	POWER	5VDC for digital logic
3	GND	POWER	Signal and DC current return
4	EJECT	IN	Logic level control, when asserted LOW, tray is ejected. When de-asserted (OPEN or HIGH) tray is closed.
5	TRAYSTATE0	OUT	The combined states of these signals indicate the current state of the tray and media as defined in the state diagram below.
6	TRAYSTATE1	OUT	
7	TRAYSTATE2	OUT	
8	ACTIVITY	OUT	Asserted LOW when disc activity (seek or data transfer) occurs.
9	12VDC	POWER	12VDC for motor control
10	5VDC	POWER	5VDC for digital logic
11	GND	POWER	Signal and DC current return
12	GND	POWER	Signal and DC current return
13	SPARE	-	Not connected
14	KEY		This pin is pulled from the shell in order to key the connector on the motherboard.

Figure 80. DVD Power and Control Interface Connector Pin Out – Motherboard Connector

4.1.7. Fan

This is a two-pin connector providing pulse-width modulated 12VDC to power the system cooling fan. Speed control of the fan shall be via open loop control of the voltage applied via pulse-width modulation.

The connector shall be a single-row 2.54mm-pitch header with a keyed shroud, MTA-100 P/N 640456-3 (Tyco/Amp) or equivalent.

Pin	Signal Name	Direction	Comment
1	FAN -	OUT	PWM output for the fan.
2	FAM +	POWER	12VDC for fan motor control
3	FAN -	OUT	This pin is connected directly to pin 1.

Figure 81. System Fan Connector Pin Out

The connector is a three-pin connector, but pins 1 and 3 are identical, allowing the connector to be reversed without impact on the functionality of the fan.

4.2. System Fan Assembly

The System Fan Assembly includes a cable harness and connector to mate with a matching receptacle on the motherboard assembly. Note that the pin out specifies only two of the three pins terminated. This arrangement allows for reverse installation at the motherboard without affecting functionality.

The connector type shall be an MTA-100 P/N 643816-3 (Tyco/AMP) or equivalent, to mate with the Fan connector described in the previous paragraph.

Pin	Signal Name	Direction	Comment
1	FAN -	POWER	PWM output for the fan.
2	FAM +	POWER	12VDC for fan motor control
3	Empty	-	This pin is left open.

Figure 82. System Fan Assembly Connector Pin Out

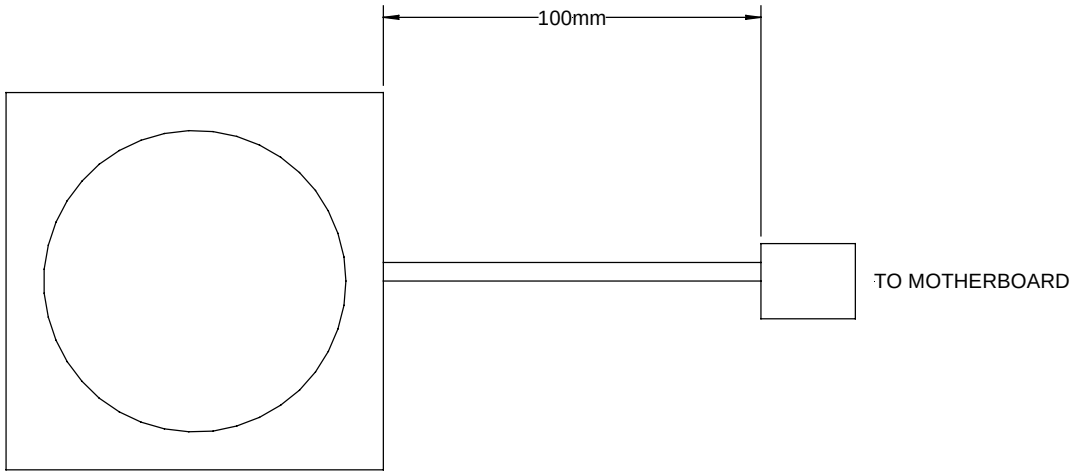


Figure 83. System Fan Assembly

Note:

A detailed specification of the fan is pending conclusion of the thermal solution.

4.3. Front Panel IO Subassembly

The front panel IO subassembly consists of a cable harness and a PCBA containing the POWER button, EJECT button, and the front-panel LED indicator. The circuit for the PCBA is described in section 2.7.4. The PCBA is electrically connected to the Front Panel IO Header on the motherboard via a cable assembly.

The PCBA and cable assembly are described in detail in the document entitled *Mechanical Design Specification, Candyland Control PCBA*.

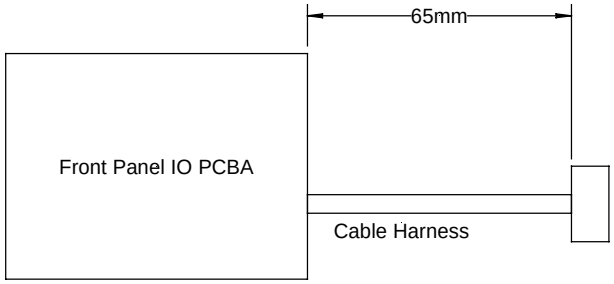


Figure 84. Front Panel IO Subassembly

The cable harness consists of an 8-conductor cable and receptacle matching the FPIO connector on the motherboard, described in section 4.1.5 with a pin out as described in Figure 56. If the harness is not directly soldered to the PCBA, then the harness shall be interfaced to the PCBA

using a connector of the same type and pin out as used on the motherboard. The wire type shall be UL type 1007, 1061, 1569 or equivalent.

4.4. Dual Controller Port Subassembly

The dual controller subassembly consists of a dual-port connector, a cable harness, and a receptacle that mates to a header on the motherboard.

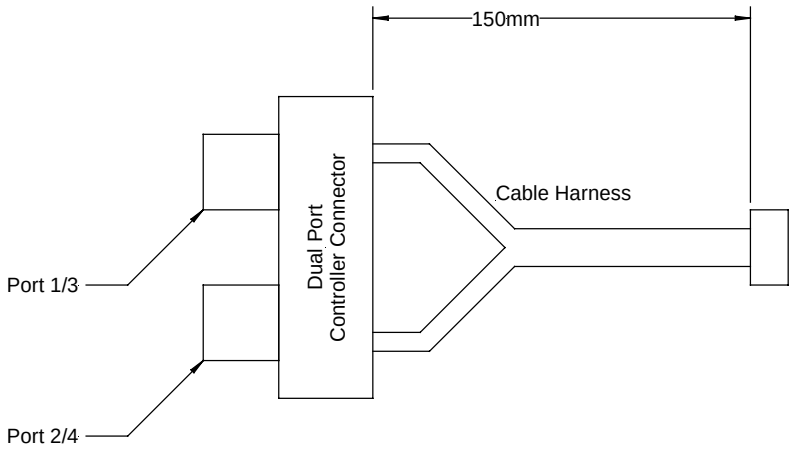


Figure 85. Dual Controller Port Subassembly

The cable harness consists of a 11-conductor cable and receptacle matching the Controller 1/2 and Controller 3/4 connectors on the motherboard, described in section 4.1.3 and 4.1.4, with a pin out as described in Figure 74. The wire type shall be UL type 1007, 1061, 1569 or equivalent.

This assembly is described in detail in the document entitle *Dual PUSB Cable Harness*.

4.5. System PSU

The System Power Supply Unit (PSU) is fully described in the *Power Supply Design Specification* for Xbox. Refer to that document for the mechanical form factor.

4.5.1. System Power

The PSU provides power to the system motherboard PCBA via a flying-lead wire to PCB interconnect. The connector shall be Molex part number 09-50-3121 or equivalent. A drawing of this connector is shown below; refer to section 4.1.1 for a pin out of this connector.

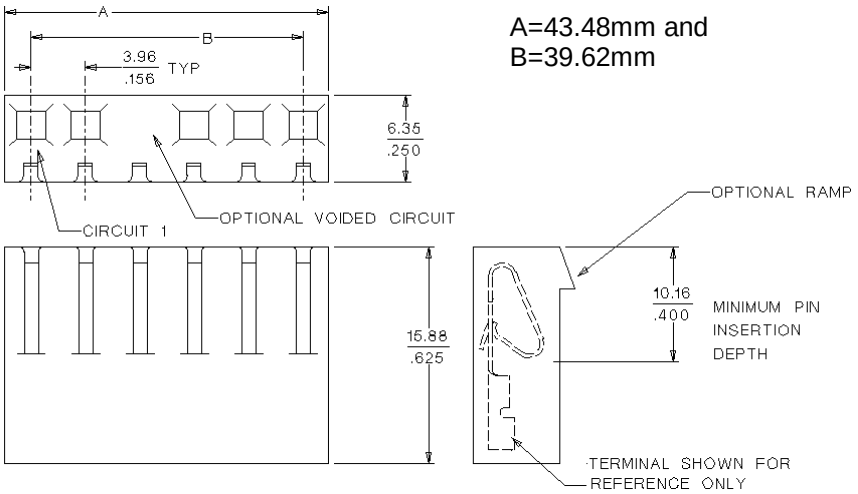


Figure 86. System Power Output Connector Header

4.5.2. HDD Power Harness

The PSU provides power to a hard disk drive via a standard 4-pin disk drive power connector harness conforming to ANSI SFF-8012, Molex Series 8981 (p/n 15-24-2000) or equivalent. A drawing of this connector is shown below.

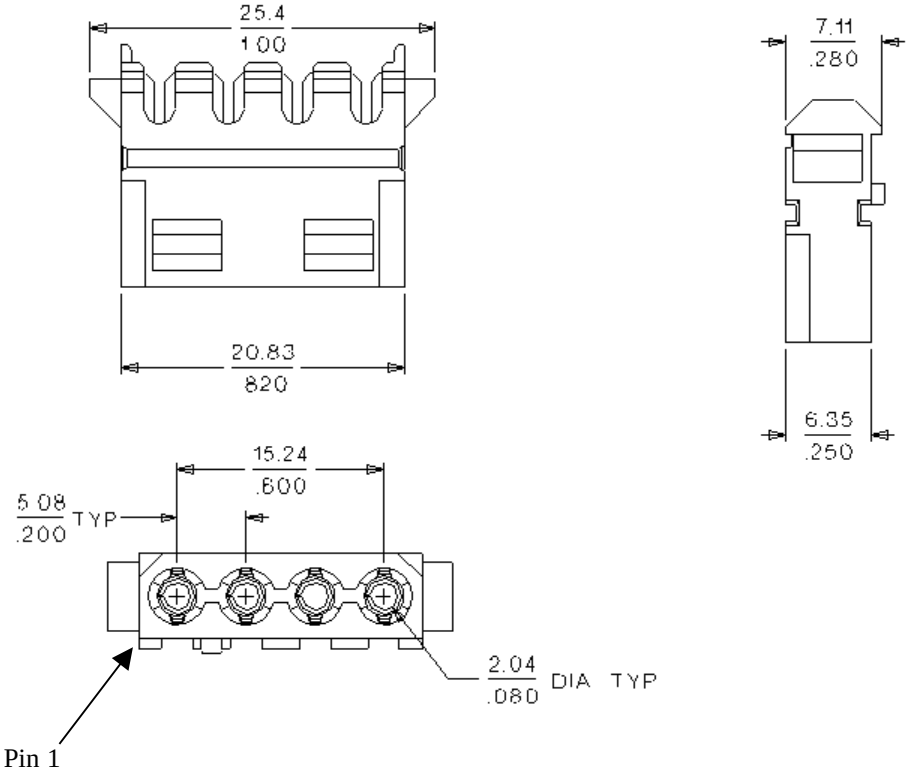


Figure 87. Disk Drive Power Connector

The pin out of this connector is shown below:

Pin	Signal Name
1	+12VDC
2	+12V Return
3	+5V Return
4	+5VDC

Figure 88. Disk Drive Power Connector Pin Out

4.6. DVD Drive

Refer to section 2.8 for a complete description of the DVD drive assembly. This drive has two interface port connectors. The ATA connector interfaces to the motherboard and provides the ATA interface signals for data transfer and drive control.

A second connector port contains the power and transport controls and status out of the drive to the system management controller.

4.6.1. ATA Connector

This connector conforms to the standard 40-pin AT-Attachment Connector specified in ANSI SFF-8059. The connector pin-out is described in section 2.9.5.1 Figure 24.

The header is keyed by removal of pin 20.

4.6.2. Power/Control Connector

This connector is fully described in section 2.9.5.2.

4.7. DVD Power/Control Cable Assembly

This cable assembly interfaces the DVD drive power and control port to the motherboard.

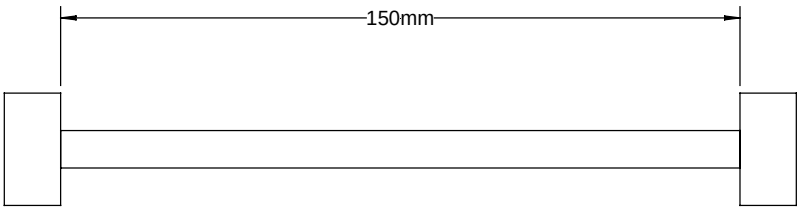


Figure 89. DVD Power/Control Cable Assembly

The cable harness consists of an 11-conductor cable terminated at both ends with 12-station receptacles matching the headers described in sections 4.1.6 and 2.9.5.The wire type shall be UL type 1007, 1061, 1569 or equivalent.

The receptacles are wired pin to pin, with pin 12 left open for keying.

Individual wire colors are TBD.

4.8. Hard Disk Drive

Refer to section 2.9 for a complete description of the hard disk drive component. The drive includes an ATA interface cable and a standard power port as described below.

4.8.1. ATA Connector

This connector conforms to the standard 40-pin AT-Attachment Connector specified in ANSI SFF-8059. The connector pin-out is described in section 2.9.5.1 Figure 24.

The header is keyed by removal of pin 20.

4.8.2. Power Connector

The HDD includes a standard 4-pin power connector receptacle conforming to ANSI SFF-8012.

4.9. ATA Cable Assembly

The ATA cable shall be a single daisy-chained assembly as shown in the drawing below:

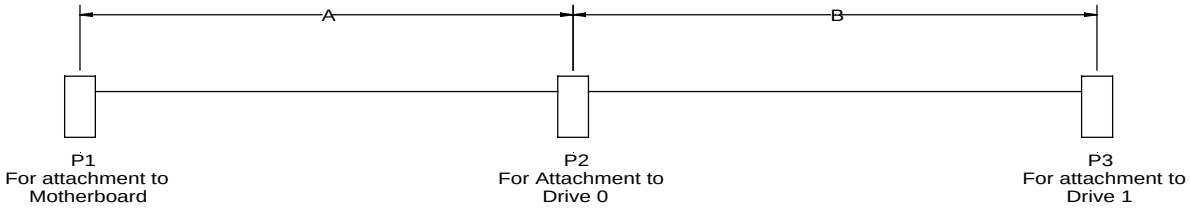


Figure 90. ATA Cable Assembly Drawing

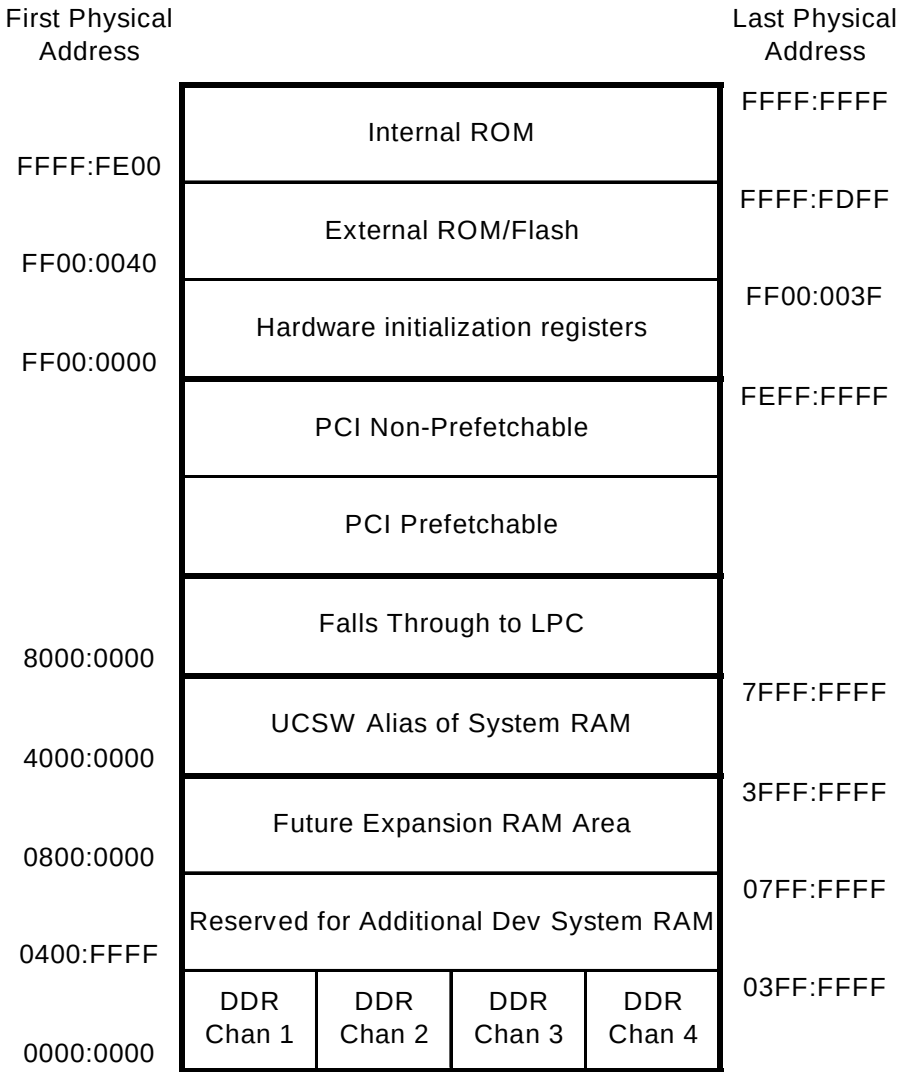
Parameter	Min	Typical	Max	Unit
Dimension “A” Distance from motherboard to DVD drive		186		mm
Dimension “B” Distance from first drive to second drive		372		mm

Figure 91. ATA Cable Dimensions

Appendix A – Power Budget Spreadsheet

Functional Block	Nom Voltage (V)	Max Current (A)	Peak Power (W)	Derate (%)	Ave Power (W)	Ave Heat (W)	Local Switch-Mode VREGs						Local Linear Vregs								System Power Supply					
							1.50		1.7		1.25		1.5		2.5		3.3		5		12		5		3.3	
							Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave	Pk	Ave
CPU																										
Core Vcc	1.7	14.6	24.8	70%	17.4	18.5			14.6	10.2																
Bus Termination	1.5	1.5	2.3	50%	1.1								1.5	0.8												
North Bridge and GPU (NV2A)																										
Core Vcc	1.50	7.0	10.5	100%	10.5	15.8	7.0	7.0																		
CPU Interface	1.7	0.60	1.0	100%	1.0				0.6	0.6																
DDR IO	2.5	1.5	3.8	100%	3.8										1.5	1.5										
LDT Supply	1.50	0.35	0.53	100%	0.5		0.4	0.4																		
Core Logic (MCPX)																										
Core Vcc	1.50	1.0	1.5	100%	1.5	2.7	1.0	1.0																		
IO Vcc	3.3	0.20	0.66	100%	0.7																				0.20	0.20
LDT Supply	1.50	0.35	0.53	100%	0.5		0.4	0.4																		
System Memory (4 Banks DDR)																										
Core Vcc and IO	2.5	2.86	7.2	77%	5.5	5.5									2.9	2.2										
Bus Termination	1.25	4	5.0	50%	2.5						4.0	2.0														
Audio DAC																										
AC-97 Digital 3.3V	3.3	0.05	0.2	100%	0.2	0.42																			0.05	0.05
AC-97 Analog 5V	5	0.05	0.3	100%	0.3														0.050	0.050						
TV Encoder (CX25871)																										
VCC Core	3.3	0.2	0.7	100%	0.7	0.9											0.2	0.2								
VCC IO	1.2	0.2	0.2	100%	0.2																					
Hard Disk Drive																										
Logic Supply	5	0.6	3.0	83%	2.5	5.6																0.60	0.50			
Motor Sypply	12	2	24.0	13%	3.1																2.0	0.3				
DVD Drive																										
Logic Supply	5	1	5.0	80%	4.0	9.8																1.00	0.80			
Motor Supply	12	1.3	15.6	37%	5.8																1.3	0.48				
Boot ROM																										
Core Vcc, Read mode	3.3	0.020	0.066	100%	0.066	0.066																			0.02	0.02
System Controller																										
Microcontroller	3.3	0.010	0.033	100%	0.033	0.033																			0.010	0.010
Temp Sensor	3.3	0.001	0.003	100%	0.003	0.003																			0.001	0.001
System Fan	12	0.300	3.600	100%	3.600	3.600															0.3	0.3				
Front Panel IO	3.3	0.050	0.165	100%	0.165	0.165																			0.050	0.050
Clock Generator	3.3	0.030	0.099	100%	0.099	0.099																			0.030	0.030
Network Interface																										
Ethernet PHY	3.3	0.18	0.6	100%	0.6	0.6																			0.18	0.18
External Power Consumption																										
Controller Port 1	5	0.5	2.5	100%	2.5	11.3																	0.5	0.5		
Controller Port 2	5	0.5	2.5	100%	2.5																		0.5	0.5		
Controller Port 3	5	0.5	2.5	100%	2.5																		0.5	0.5		
Controller Port 4	5	0.5	2.5	100%	2.5																		0.5	0.5		
AVIP Power	5	0.25	1.3	100%	1.3														0.25	0.25						
Local Vreg Controllers																										
ADP3158	12	0.057	0.7	100%	0.7	13.1															0.057	0.057				
SC1110	12	0.057	0.7	100%	0.7	0.0															0.057	0.057				
SC1103	12	0.150	1.8	100%	1.8	18.4															0.150	0.150				
Local Switch-Mode Vreg																										
1.5V (NV2A and MCPX)	5	3.63	18.1	100%	18.1	5.1																	3.6	3.6		
1.7V (CPU)	5	6.71	33.6	71%	23.9	5.5																	6.7	4.8		
1.25 (DDR Vtt)	5	1.18	5.9	50%	2.9	0.4																	1.2	0.6		
Local Linear Vreg																										
1.5V (CPU Vtt)	3.3	1.5	5.0	50%	2.5	1.4																			1.5	0.8
2.5V (DDR)	3.3	4.4	14.4	85%	12.3	3.0																			4.4	3.7
3.3V Analog	5	0.2	1.0	100%	1.0	0.34																	0.2	0.2		
5V Analog	12	0.3	3.6	100%	3.6	2.1															0.3	0.3				
Peak Current (A)							8.7		15.2		4.0		1.5		4.4		0.20		0.30		4.2		15.3		6.4	
Average Current (A)							8.7		10.8		2.0		0.8		3.7		0.20		0.30		1.6		12.5		5.0	
Power Supply Design Limits (A)							9.6		16.8		4.4		1.7		4.9		0.30		0.40		4.6		16.9		7.1	
Peak Power Output (W)							13.1		25.8		5.0		2.3		10.9		0.66		1.5		50.0		76.6		21.1	
																					148					
Continuous Power Output (W)							13.1		18.4		2.5		1.1		9.3		0.66		1.5		19.3		62.5		16.5	
																					98.2					
Efficiency (%)							72.0%		77.0%		85.0%		45.5%		75.8%		66.0%		41.7%		80%					
Average Heat Dissipation (W)							5.1		5.5		0.4		1.4		3.0		0.34		2.1		**24.6**					
Total Average System Heat Dissipation (W)							**137.6**																			

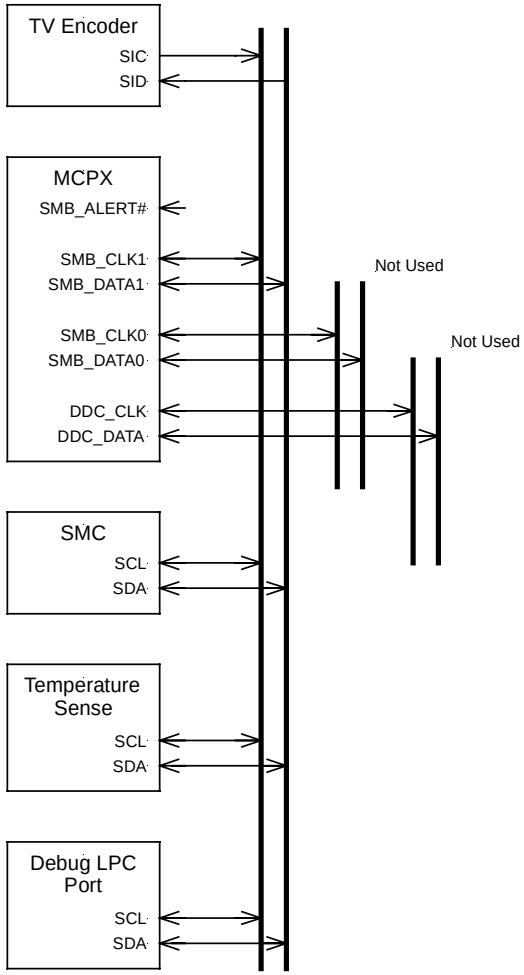
Appendix B – System Memory Map



Appendix C – SM Bus Address Map

All SMBus devices in Xbox share a single bus. The SMC and the MCPX both act as master devices on the bus, each capable of initiating bus transactions. The two other devices on the bus are the TV Encoder and the Temperature sensor. The figures below show the interconnection and the address map for the SMBus.

SM Bus Address Map		
Device	**Direction**	**Address**
MCPX	W R	0x10 0x11
TV Encoder	W R	0x88 0x89
System Micro Controller	W R	0x20 0x21
Temperature Measurement	W R	0x98 0x99



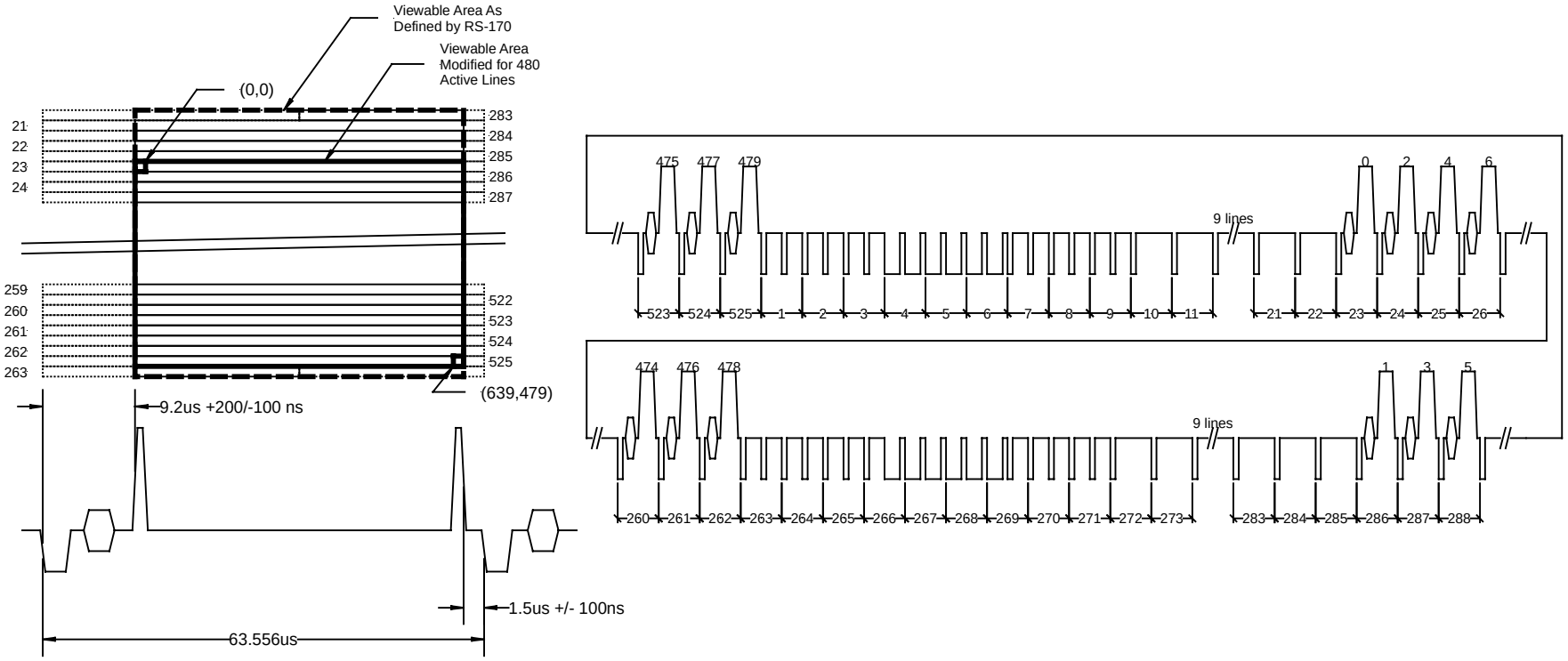
Appendix D – Television Systems Used By Country

Country	Television System	Lines	Field Rate (Hz)
United States	M / NTSC	525	59.94
Canada	M / NTSC	525	59.94
Mexico	M / NTSC	525	59.94
Japan	M / NTSC	525	59.94
United Kingdom	I / PAL	625	50
Ireland	I / PAL	625	50
France	L / SECAM	625	50
Germany	B / PAL G / PAL	625	50
Spain	B / PAL G / PAL	625	50
Italy	B / PAL G / PAL	625	50
Belgium	B / PAL H / PAL	625	50
Netherlands	B / PAL G / PAL	625	50
Luxembourg	B / PAL G / PAL SECAM-L	625	50
Norway	B / PAL G / PAL	625	50
Sweden	B / PAL G / PAL	625	50
Finland	B / PAL G / PAL	625	50
Australia	B / PAL G / PAL	625	50
New Zealand	B / PAL G / PAL	625	50

Source: ITU-R BT.470-4 Appendix I to Annex I

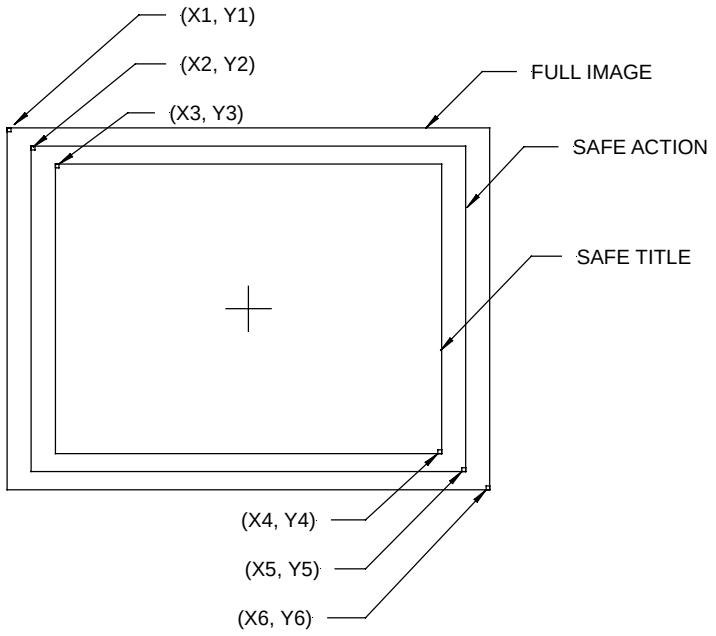
Appendix E – Video Waveform Timing

480-line NTSC Waveforms (640x480)



Appendix F – Safe Action and Safe Title Guidelines

Frame Mode	Full Image				Safe Action				Safe Title			
	X1	Y1	X6	Y6	X2	Y2	X5	Y5	X3	Y3	X4	Y4
640x480	0	0	639	479	32	24	608	456	64	48	576	432
720x480	0	0	719	479	36	24	684	456	72	48	648	432



Appendix G – System RESET Flow Control

The Xbox system reset is controlled by three possible events:

User Command (Power on, Eject)

Power Supply (POWOK)

Software (Self-Reset)

From the power off condition, power on is initiated by the user pressing either the POWER or EJECT buttons. This input is received by the SMC, which in turn asserts the POWON signal to the PSU and begins monitoring the POWOK signal. The SYSRESET signal having been asserted in the low state up to this time, SYSRESET is deasserted after POWOK is asserted by the PSU.

The SYSRESET signal from the SMC drives the two power-good signals into the MCPX (POWGD and POWGD_SB) as well as the POWGOOD input to the CPU. While the MCPX signals are asserted, the MCPX holds PCI_RESET# asserted, which drives the RESET# input of the NV2A GPU. While RESET# is asserted into the NV2A, the NV2A holds the CPU in a reset state by asserting the CPU_RST# output driving RESET# into the CPU.

After the MCPX initializes, it deasserts PCI_RST#, allowing the NV2A to initialize and in turn deasserts RESET# into the CPU.

The figure that follows shows this flow of signals as described, and the relative order of events that occurs from power on to system reset complete.

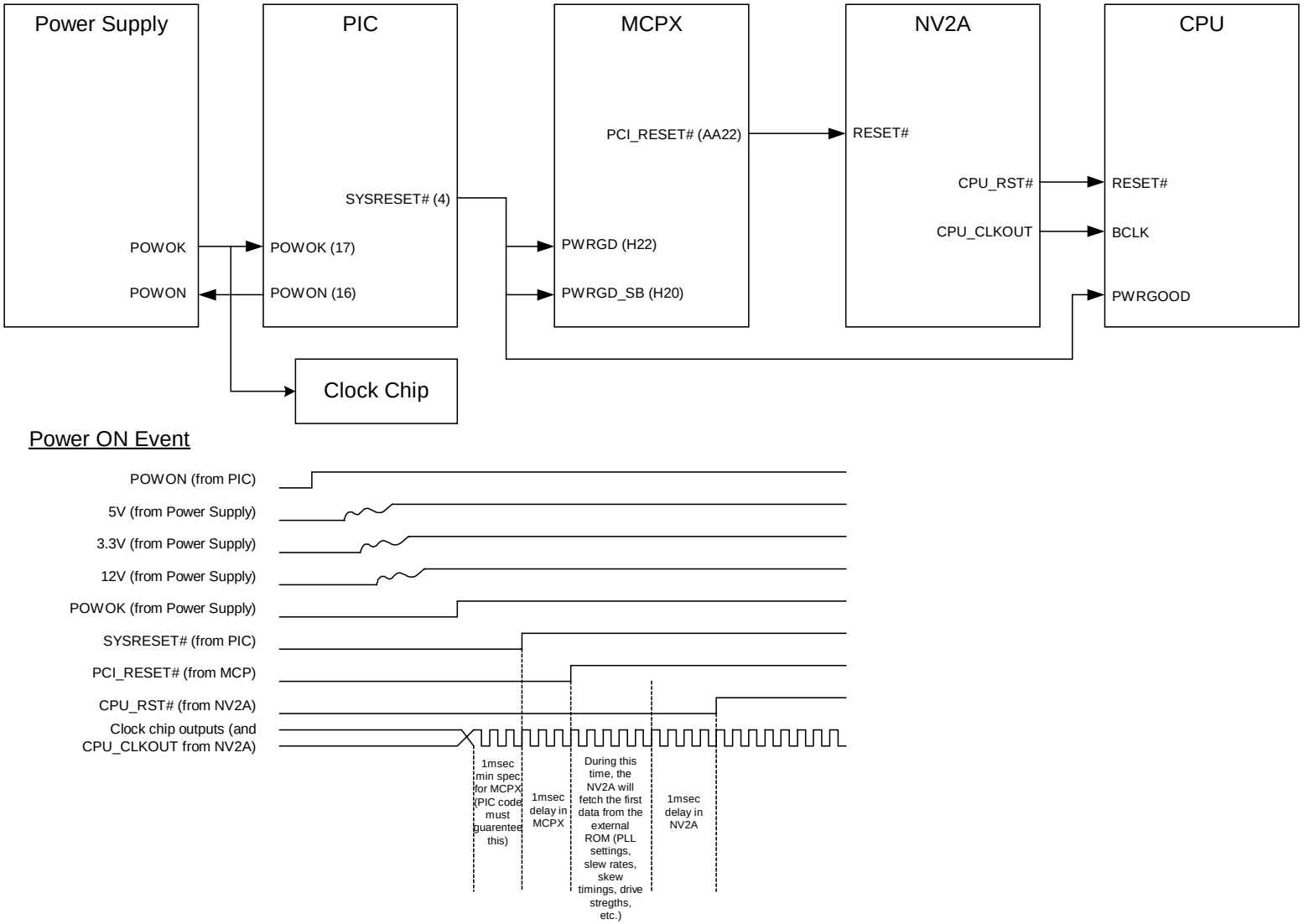


Figure 92. System RESET Control Flow

Note that from the POWON condition, the SMC will initiate RESET if either standby power is lost, or POWOK is deasserted by the PSU. Similarly, the SMC will initiate a RESET sequence if the user manually presses the POWER switch. A reset cycle may also be initiated by software by manipulating register values in the MCPX as described in the MCPX data sheet or by requesting a system power down through the SMC.